MODEL 532
OPERATION MANUAL

MODEL 532

Intelligent Logic State Analyzer

OPERATION MANUAL

PARATRONICS INC.

IMPORTANT!

MODEL 532 OPERATION MANUAL UPDATE FORM

From time to time, additional technical and applications information concerning the Model 532 will become available. Please fill out the form below to get on the mailing list.

(detach here)

AFFIX
1ST CLASS
POSTAGE

Paratronics, Inc.
800 Charcot Avenue
San Jose, CA 95131

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USER'S NAME _____ TITLE _____

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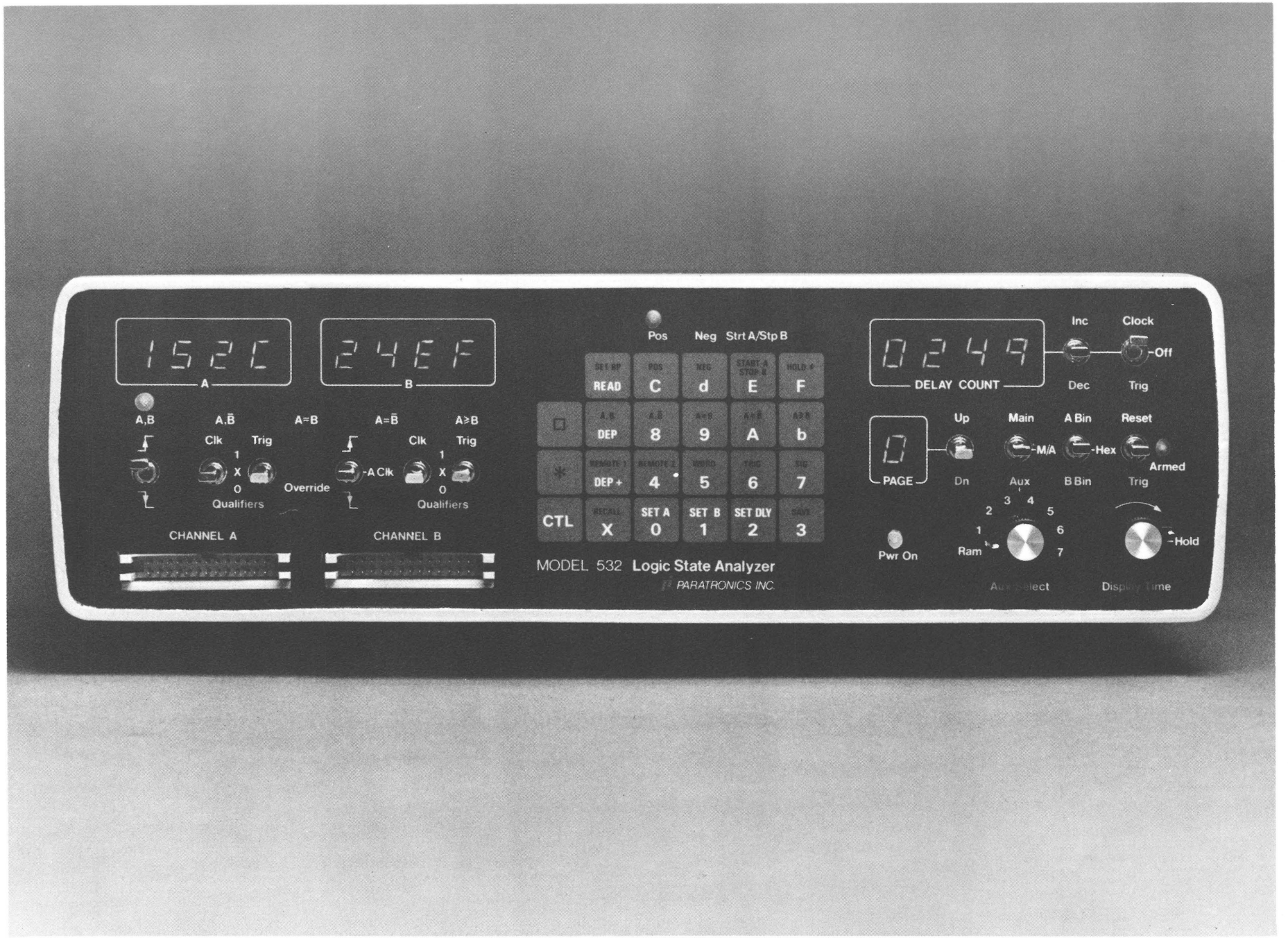
1 5 2 C
A
2 4 E F
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A,B
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Clk
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Qualifiers
A=B
Override
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A Clk
A≥B
CHANNEL A
CHANNEL B
Pos
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Strt A/Stp B
READ
C
d
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DEP
8
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A
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DEP+
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CTL
RECALL
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SET A
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1
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SAVE
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MODEL 532 Logic State Analyzer
PARATRONICS INC.
0 2 4 9
DELAY COUNT
Inc
Clock
Dec
Off
Trig
0
PAGE
Up
Dn
Main
M/A
Aux
A Bin
Hex
B Bin
Reset
Armed
Trig
Pwr On
Ram
1
2
3
4
5
6
7
Hold
Aux Select
Display Time

	-A-	-B-
SELF TEST SIGNATURE	5597 (4-digit HEX code)	100F (4-digit HEX code)

(Transfer from test tag on line cord upon unpacking unit.)

PDP-11 PROBE = COMP

~~MODE A/B NEG~~

A TRIG — N XX

WARNING

DO NOT REMOVE TOP COVER UNLESS THE AC LINE CORD IS FIRST UNPLUGGED.

SERVICE OF THIS INSTRUMENT SHOULD ONLY BE PERFORMED BY SKILLED MAINTENANCE PERSONNEL.

NOTES

1. THE RESET/TRIG SWITCH AT THE RIGHT OF THE FRONT PANEL MUST MOMENTARILY BE PLACED IN THE RESET POSITION EACH TIME THE MODEL 532 IS POWERED UP. THIS ACTION DISABLES THE AUTOMATIC SELF TEST.
2. A SPARE INPUT BUFFER IS TAPED TO THE INSIDE OF EACH MODEL 50 DATA INPUT PROBE.

APPLICABLE DOCUMENTS:

Model 532 Maintenance Manual

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1.0 INTRODUCTION

You now own the most versatile logic state analyzer available. The Model 532 is unique among analyzers in that it combines a number of sophisticated features never before offered in a single digital test instrument.

With the Model 532, the user can:

* Monitor up to 32 channels at rates up to 12 MHz; or 16 channels at rates up to 24 MHz.

* Capture 250 states before or after the trigger word.

* Operate the instrument alone, with an ordinary oscilloscope, or with an RS-232/TTY terminal.

* Display data in hexadecimal or binary.

* Choose from among 21 powerful triggering modes, including triggering on the nonoccurrence of an expected event.

* Read the signature of the data collected.

* Demultiplex address and data on a multiplexed bus.

* Program the instrument for automatic testing or special applications.

* Remotely control product testing, including over the telephone lines.

* Obtain a hardcopy of test results.

* Support microprocessor system development.

These features assure the user that the Model 532 will not be obsoleted for years to come...in spite of rapid advances in microprocessor technology. Fig. 1-1 illustrates some of the equipment the analyzer can interface with to support most testing requirements.

Although capable of analyzing complex problems, the Model 532 offers several features which simplify its use. Without these simplifying features, the user could spend a great deal of time connecting the unit to the system-under-test, setting up the desired triggering mode, and finally, examining the collected data.

The Model 532 simplifies interfacing using two 16-bit probes for direct connection to mating "test ports" on the system-under-test. For systems lacking such ports, the Model 532 package includes a probe terminator assembly with color-coded flying leads. At the end of these leads are spring-loaded pins which readily mate with IC clips, wirewrap pins, or E-Z hooks. Section 7.0, "Connection to the System-Under-Test," discusses the various interconnection techniques in detail.

For triggering mode selection, the Model 532 incorporates a calculator-type keyboard. Indicator lights tell the user at a glance which mode has been selected. Section 4.0 "Description of Controls, Indicators and Connectors" and Section 8.0 "Triggering Modes," discuss these modes in detail.

Another operational simplification results from the use of the Model 532's optional Auxiliary Memory Board. Each of the eight memory elements on the board is capable of accepting an entire 32-bit, 250-word data collection from main memory--as well as the front panel settings used to make the collection. Later, when one of the auxiliary memory elements is activated, the stored front panel settings are recalled and another data collection is automatically initiated. When this collection is complete, the new data now in the main memory are automatically compared with old data stored in the auxiliary memory and and differences are flashed on the CRT. Section 9.0, "Typical Logic State Analysis Applications" describes how this and other features can be used in R&D, field service, and production test applications.

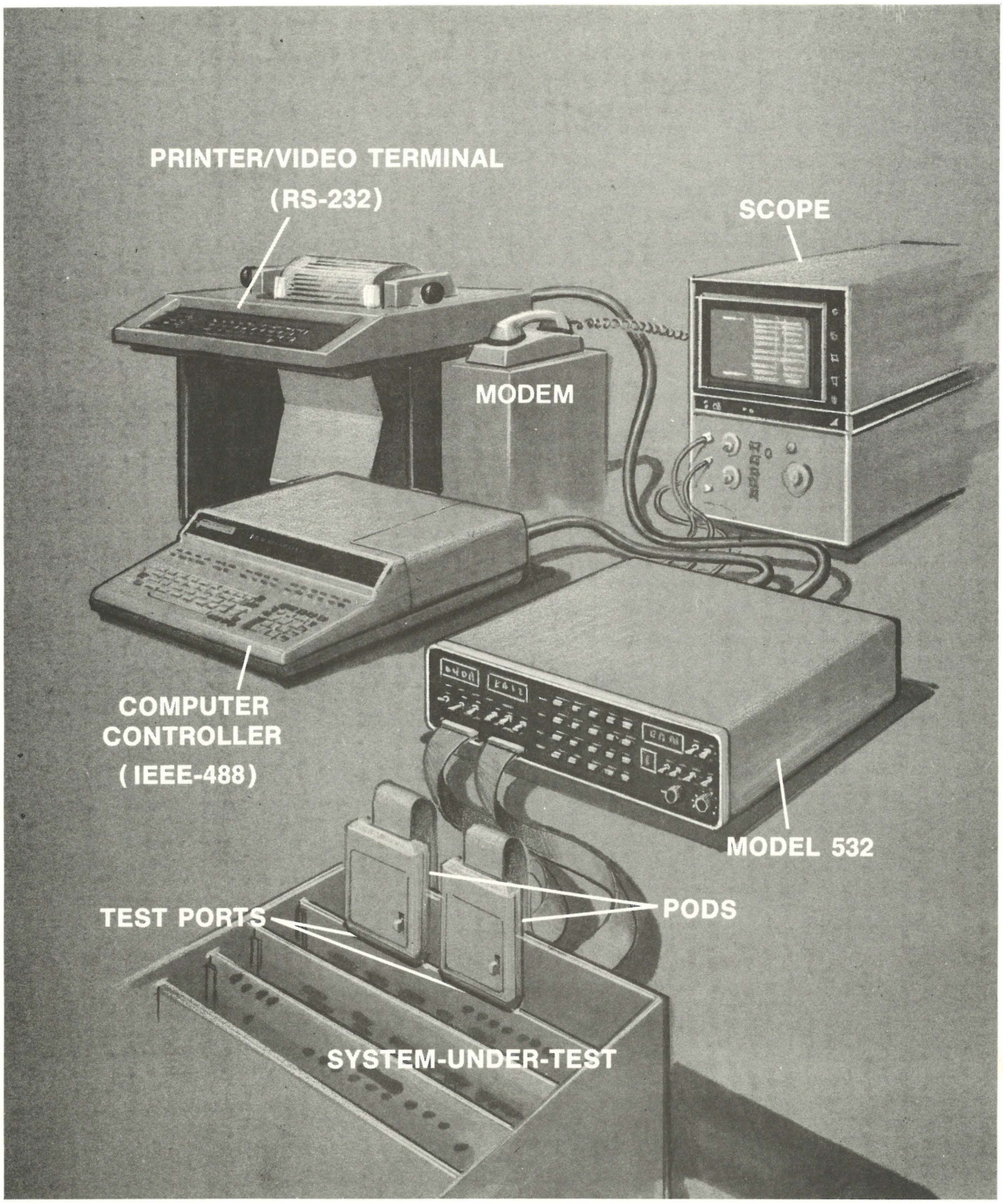


Fig. 1-1. The Model 532 has the interfaces required to support most testing requirements.

In order to reduce the time it takes to analyze the large amount of data collected by the Model 532, the instrument also incorporates a "signature analysis" capability as a standard feature. Note that this technique is not the same one used in the HP-5004A Signature Analyzer in that it does not require that the system-under-test contain special hardware and software to support it. It is best described as a data reduction technique which operates on the 32-bit data in the Model 532's main memory and "compresses" it into two 4-digit hexadecimal signatures, where each signature represents a 16-bit vertical slice of the memory contents. Thus, if two data collections are different, even by one bit, the associated signatures will also be different. This feature can save the user a great deal of time particularly when a test requires a series of sequential data collections in search for an intermittent state--only the signatures need be compared to determine if the erroneous state is contained in the latest collection. The Model 532's signature analysis feature is further described in Appendix A.6.

Besides the powerful test support provided by the Model 532 in its capacity as an Intelligent Logic State Analyzer, the instrument also performs several functions which are somewhat outside the strict definition of the term "logic state analyzer." With its optional serial RS-232C/TTY and IEEE-488 interfaces, the Model 532 can operate in an ATE (Automatic Test Equipment) capacity as shown in Fig. 1-1. The serial interface permits a hardcopy printout of test results, control of the unit using a video terminal or teletype keyboard, and even remote control and analysis over the telephone lines. The IEEE-488 interface permits a broad series of automatic tests to be performed under the direction of an external controller.

Another application considered to be outside the domain of the general-purpose logic state analyzer is microprocessor system development. (The logic state analyzer has historically been a passive test instrument for capturing data while microprocessor development tools have provided active functions such as READ/WRITE, SINGLE STEP, HALT, RUN, BREAKPOINT, etc.) With special probes, each dedicated to the particular microprocessor chip being used, the Model 532 can perform development functions as well. Section 11.0, "Microprocessor System Development Applications" describes how the Model 532 can support software and hardware development with the active control functions mentioned above.

In summary, the inherent versatility of the Model 532 permits its use in all phases of a product's lifecycle. In the lab, for example, its monitoring capability, powerful triggering modes, dual-clocking, high-speed operation, and development system functions make the Model 532 useful in support of even the most advanced product design. Then, when the development phase is complete, the GO/NO-GO aspect of signature analysis, the automatic computer-control capability, and the hardcopy printout option make the Model 532 useful in production test. And, finally, when the product is in the field, the Model 532's compact size, its seven pre-programmed on-board tests, and its remote diagnosis feature make the instrument the logical choice in field service as well.

In order to get the most out of the Model 532, the reader should review this entire manual. After reviewing the material, if technical questions arise, feel free to contact any member of the engineering staff at Paratronics, Inc. or an applications engineer at your local Paratronics, Inc. sales office. Note that a separate maintenance manual is also available for troubleshooting, calibration, and maintenance information.

2.0 SPECIFICATIONS

Physical
8.9 cm (3½") high x 30.9 cm (12⅛") wide x 36.2 cm (14¼") deep; 4.4 kg. (9¾ pounds)

Display
Trigger word, data, signatures, page indicator and digital delay relative to trigger on self-contained LED readouts; or oscilloscope display provides same information along with data in sixteen selectable 16-line hexadecimal or binary truth table "pages."

Real-Time Data Collection
250 words, each 32 bits wide. Data memory organized as two 16-bit data groups (A and B). Each data group has independent input clocks and trigger and clock qualifiers.

Input Clocks
Maximum clock rate is 5 MHz with standard memory or 12 MHz with optional high-speed memory. Rising or falling clock edge can be selected independently for A or B group; or both groups can be clocked together from A clock. Minimum clock pulse width is 20 ns at threshold.

Oscilloscope Requirements
Input sensitivity (X and Y): 1V/division min.; bandwidth: 500 KHz min.; X, Y phase shift: ≤ 10° at 300 KHz; blanking (Z axis): fully blanked by positive or negative pulse, 30V or less. Analyzer provides required X, Y, Z outputs using BNC connectors at rear of unit.

External Sync Output
BNC connector at rear of unit provides TTL pulse when all triggering requirements are met.

Trigger Bus
Connector at rear of unit expands analyzer triggering beyond 32 bits.

RS-232C/TTY and IEEE-488 Outputs
Standard connectors at rear of unit for two-way communication and control functions.

Probes: 107 cm (3.5') long

Fixed Threshold Type (1.6V): All inputs have one low-power Schottky load as follows: −400ua max. (−0.5V to +0.9V); +100ua max (+2.0V to +15.0V). Inputs incorporate 400mV min. hysteresis for noise rejection. Input capacitance < 20pF at probe head. Switch on probe inverts (compliments) all data and qualifiers. Probe accepts terminator with color-coded "flying" leads or plugs directly into system at test port.

Variable Threshold Type (±15.0V range): All inputs have 50K Ω, 15pF input impedance. Fixed TTL threshold (1.6V) is also provided. Probe interfaces with system-under-test as described above.

Dedicated Probe: Input load same as Fixed Threshold Type. Probe interfaces with microprocessor socket using dedicated 40-pin DIP plug and provides SINGLE STEP, RUN, HALT, BREAKPOINT, and memory READ/WRITE and other development functions.

Qualifiers
Both trigger and clock qualifiers are provided for each 16-bit group. Qualifiers can be independently set to 1, 0, or X (don't care).

Set-Up and Hold Times
Set-up time for data and qualifiers prior to selected clock edge is 30 ns. Hold time for data and qualifiers after selected clock edge is 0 ns.

Delay
Up to 10,000 clock or trigger events.

Triggering Modes
General: Analyzer triggering is specified by the A and B data groups. Each group is defined by keyboard entry of 0 to 4 hexadecimal characters. Provides pre-trigger and post-trigger data capture. Delay, if any, can be on n trigger or clock events, where $0 \leq n \leq 9999$.

Parallel Modes: (A,B) refers to a full 32-bit wide trigger word. (A,B)DLY: Trigger when (A,B) occurs and delay condition is satisfied. (A,$\bar{B}$)DLY: Trigger when A and any word other than B occurs and delay condition is satisfied.

Sequential Modes: (A=B) refers to two trigger words in the A data group. A is the trigger word that must occur first; B is the trigger word that must occur second. In this mode, the B data inputs have no effect on triggering. Full 32-bit data collection and display still occurs.

(A,DLY=B): Trigger when B occurs exactly n clock or trigger delay events from A.

(A,DLY=$\bar{B}$): Trigger when any event other than B occurs exactly n clock or trigger delay events from A.

(A,DLY ≥ B): Trigger when B occurs n or more delay events from A.

Start A/Stop B: Start data collection when A occurs; stop collection when B occurs. If more than 250 data words separate A & B, the most recent set of 250 words are stored.

Auxiliary Memory
1K RAM and 7K UV PROMs are provided. Each of the 8 memory elements is capable of storing front panel control settings for later automatic operation, 250 words of data, and associated signatures. PROMs are programmed by Model 532 only if blank and can be erased by UV light. Differences between main and auxiliary memories are highlighted on CRT by alternating displays.

Program Memory
Can be user-defined and expanded for special applications. 1K RAM plus 8K PROM are available.

Power
Analyzer uses wide-range, high-efficiency power supply: 90-240V rms AC; 48-440 Hz; 120-350 VDC; 75VA max.

Operating Temperature Range
0-50°C.

Humidity
0-95% R.H. with no condensation.

Altitude
To 10,000 feet.

Note: Paratronics, Inc. reserves the right to change specifications without notice.

3.0 UNPACKING & INSPECTION

Important: As soon as the equipment is unpacked, make certain to record the self-test signature pair printed on the test tag (located on the line cord) in the space provided at the front of this manual.

3.1 BASIC EQUIPMENT

The following is a list of items which form a basis of every shipment:

Model 532A - 5 MHz unit with MOS-type data memory

or

Model 532B - 12 MHz unit with bipolar-type data memory

The above models include the following items as standard equipment:

- 3-wire line cord
- 1.5 amp slo-blo fuse
- Model 53 self-test adaptor
- Instruction manual
- Warranty
- Shipper

3.2 OPTIONAL EQUIPMENT

The following is a list of items which are optional:

3.2.1 PROBES

A minimum of two 16-channel probes are required for 32-channel operation. One dedicated probe is required for microprocessor development applications.

* Model 50 - 16-channel fixed threshold (TTL) probe with Model 52-1 terminator.
* Model 51 - 16-channel variable threshold (±15V) probe with Model 52-1 terminator.

* Model XXXX - 40-pin microprocessor development probe. (XXXX) corresponds to type of microprocessor chip.

NOTE

A SPARE INPUT BUFFER IS TAPED TO THE INSIDE OF EACH MODEL 50 PROBE.

3.2.2 ACCESSORY BOARDS

The following option boards, if selected, are shipped installed in the instrument:

* RS-232C/TTY SIB - Serial Interface Board permitting two-way bit-serial communication and control over standard RS-232C and 20 mA current loop interfaces. (See Appendix A.3 for installation and operation.)

* IEEE-488 PIB - Parallel Interface Board permitting two-way byte-serial communication and control over standard IEEE-488 interface. (See Appendix A.4 for installation and operation.)

* Auxiliary Memory - Accessory board containing 1K of RAM, PROM programming circuitry, and 4 sockets for up to 8K of 2716 UV PROMS (7K are useable). Permits automatic testing and data storage. (2716 UV PROMS optional.)

* User's Program Memory - Similar to Auxiliary Memory board except that here all 8K of PROM are useable. Permits Model 532 to be programmed to perform enhanced microprocessor development system applications as well as user-defined functions. Two jumper wires define the address space for this board.

3.2.3 ADDITIONAL ACCESSORIES

* One or more 2716 UV PROMS (installed) - UV erasable, single supply voltage memory chips for use with the Auxiliary and User's Program Memory Boards.

* Maintenance Manual - Provides schematics, calibration, testing, maintenance, and troubleshooting information.

* Additional Model 52 Terminators - Several connected to system-under-test permit rapid interfacing of analyzer probes in order to increase amount of data monitored.

3.3 VERIFICATION OF ORDER

The user should check the original purchase order, the shipper, and the test tag located on the line cord to ensure that the proper equipment configuration has been received. To check for optional Accessory Boards and PROMS, unlock the captive fasteners on the top cover by rotating 1/2 turn and lift and slide the top cover back.

NOTE

FROM TIME TO TIME, CERTAIN OPTIONAL ITEMS MAY BE TEMPORARILY OUT OF STOCK AND THEREFORE ARE NOT INCLUDED IN THE ORIGINAL SHIPMENT. IF YOU FIND ANY OPTIONAL EQUIPMENT MISSING, CHECK THE SHIPPER TO DETERMINE IF THE ITEM IS ON BACK ORDER. (ACCESSORIES MAY BE ADDED TO THE MODEL 532 IN THE FIELD AT ANY TIME WITHOUT AFFECTING THE BASIC PERFORMANCE CHARACTERISTICS OF THE EQUIPMENT.) BACK ORDERED OPTIONS HAVE HIGHEST PRIORITY AND WILL BE SHIPPED AS SOON AS POSSIBLE.

If an item which appears on the P.O. is missing and is not on the shipper as a back ordered item, immediately notify Paratronics, Inc., or one of our local sales offices.

3.4 INSPECTION

Once the user has verified the status of the basic equipment and options, a careful visual inspection of the equipment should be performed. Look for obvious shipping damage such as dents or punctures. Also check for loose PC boards, IC's or other components.

NOTE

IF SHIPPING DAMAGE HAS OCCURRED, SAVE THE ORIGINAL CONTAINER AND NOTIFY THE SHIPPER IMMEDIATELY.

3.5 RETURN OF EQUIPMENT

If the unit must be sent back to the factory for any reason, contact the factory or your local Paratronics, Inc. sales office for authorization.

NOTE

EQUIPMENT RETURNED TO THE FACTORY WITHOUT PRIOR AUTHORIZATION CANNOT BE ACCEPTED.

If you have authorization to return the instrument, use the original shipping container and packing material, if possible.

3.5.1 SUGGESTIONS CONCERNING RETURN OF EQUIPMENT

If you can identify the subassembly, board or component responsible for the problem, it is often more convenient to return just the faulty item rather than the entire instrument. This is particularly true for international customers. However, regardless of how you proceed, please send a brief description of the problem with the faulty item: this can speed the repair cycle.

NOTE

THE MAJORITY OF PROBLEMS RESULT FROM SUBJECTING THE DATA INPUT PROBES TO OVERVOLTAGE OR IMPROPER GROUNDING. FOR THIS REASON EACH MODEL 50 PROBE CONTAINS A SPARE INPUT BUFFER TAPED TO THE INSIDE OF THE CASE. USE OF THIS BUFFER CAN SAVE YOU THE INCONVENIENCE OF RETURNING THE PROBE TO THE FACTORY.

4.0 DESCRIPTION OF CONTROLS, INDICATORS, & CONNECTORS

Although the arrangement and function of the Model 532's controls, indicators and connectors is often self-explanatory, several of these items can have multiple operating modes which may not, at first glance, seem obvious. Therefore, in order to get the most from this instrument, it is recommended that the user review this section thoroughly before attempting to use the Model 532.

4.1 GENERAL

The following description of the unique memory partitioning and the two main triggering mode categories of the Model 532 provide background material which will help the user better understand the rest of the information in this section.

4.1.1 ANALYZER MEMORY PARTITIONING

The 32-channel x 250-word-deep data memory of the Model 532 is actually vertically partitioned into two 16-channel by 250-word sections, called the A data channels and B data channels--or A and B for short. Each A and B section collects data through the corresponding 16-channel input data probe and each section can also be clocked and qualified independently of the other. (See Fig. 4.1.1-1.)

4.1.2 TRIGGERING MODES

The Model 532 has two main catagories of triggering modes: PARALLEL and SEQUENTIAL.

4.1.2.1 PARALLEL TRIGGERING MODE

This mode refers to a single trigger word that can be up to 32 bits wide. Here, A refers to a 16-bit trigger and in the A data channel and B refers to a 16-bit trigger word in the B data channel. To form the trigger word, A and B are paralleled.

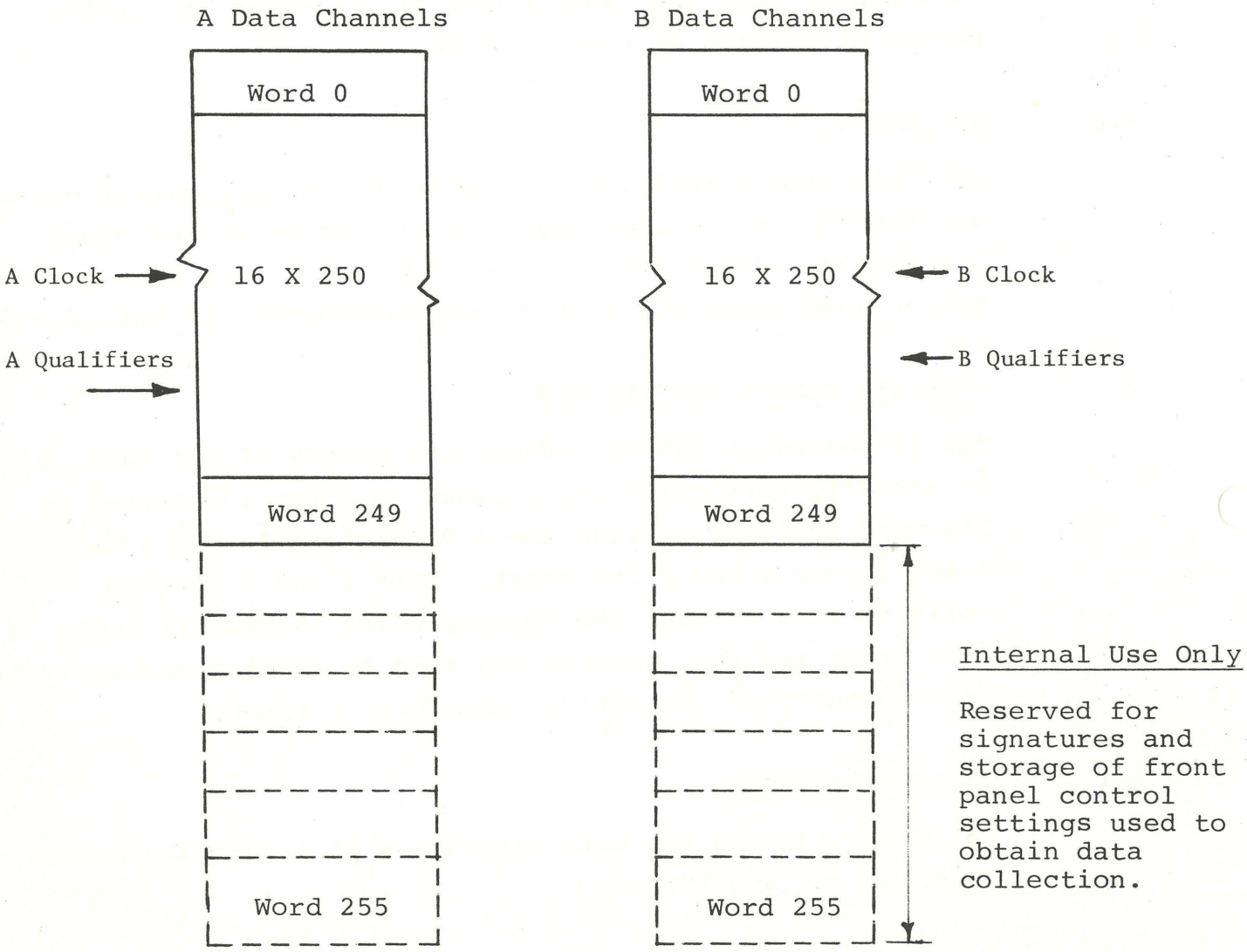


Fig. 4.1.1-1. Model 532 memory partitioning.

4.1.2.2 SEQUENTIAL TRIGGERING MODE

This mode refers to two sequential trigger words, each up to 16 bits wide. Here, A refers to the first word which must occur in the A data channel and B now refers to the second 16-bit-word which must also occur in the A data channel. B is always separated from A by a predefined number of events, such as program steps or loops.

4.2 FRONT PANEL

The front panel is shown in Fig. 4.2-1.

4.2.1 SEVEN-SEGMENT READOUTS

As described below, these readouts often have multiple display functions.

4.2.1.1 A DISPLAY

This readout displays A data channel information in a 4-digit hex code. Three different 16-bit words are available for display as selected from keyboard commands. The three words are:

* A Trigger Word
* A Data Word
* A Signature

4.2.1.2 B DISPLAY

Same function as above. The three 16-bit words displayed are:

* B Trigger Word (Parallel or Sequential Trigger Modes)
* B Data Word
* B Signature

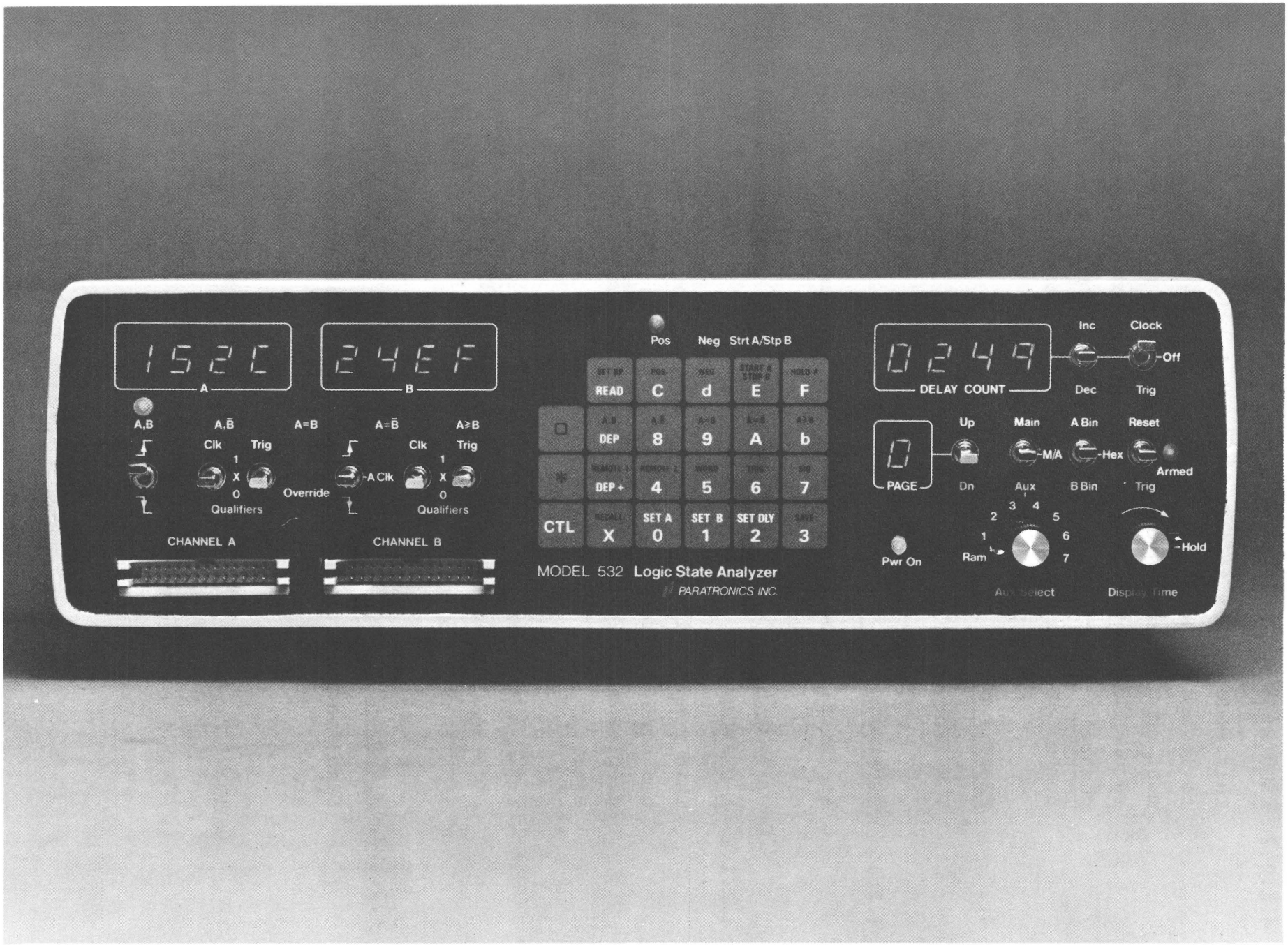


Fig. 4.2-1. Model 532 front panel.

4.2.1.3 DELAY COUNT READOUT

This 4-digit decimal display has different functions depending upon which mode the A and B displays are in:

A AND B DISPLAY MODE	DELAY COUNT DISPLAY MODE
Trigger Word	No. of clock or trigger word events (up to 9,999) which are required to satisfy triggering conditions; or when Model 532 is used in automated testing applications, the delay value indicates which remote test is being executed.
Data Word	Location of displayed word in data memory. In this word location mode, the delay value can vary between 0 and 249 (max).

Note: The value in the DELAY COUNT readout in the TRIGGER WORD mode and the value in the DATA WORD mode are maintained separately by the software so that different delay values can be used for a data collection and subsequent word display. Thus, the delay value used in the TRIGGER WORD mode represents the number of clock or trigger events which must occur prior to triggering; while the delay value in the WORD mode is simply the location of the data word in the analyzer's memory.

4.2.1.4 PAGE

This single-digit readout indicates to the operator which of sixteen binary or hexadecimal truth tables is currently selected for display on the CRT. Note the following important definition: PAGE 0 always contains the first data words collected while PAGE F always contains the last words collected. This is true for both the POS and NEG (post-trigger and pre-trigger) display modes.

4.2.2 LED INDICATORS

These indicators generally have the single function described below.

4.2.2.1 TRIGGER MODE LED'S

There are 8 discrete LED's used to indicate the triggering modes programmed into the Model 532 by manual or automatic commands.

LED	MODE	TRIGGERING REQUIREMENTS
(A,B)	PARALLEL	A and B are paralleled to form the trigger word. (Up to 32 bits.)
(A,$\overline{B}$)	PARALLEL	A and any other word other than B are paralleled to form the trigger word. (Up to 32 bits.)
(A=B)	SEQUENTIAL	A must occur first in the A data channel; B must occur second in the A data channel, after n clock or trigger events.
(A=$\overline{B}$)	SEQUENTIAL	A must occur first in the A data channel; and any word other than B must occur second in the A data channel after n clock or trigger events.
A $\geq$ B	SEQUENTIAL	B must occur at least n clock or trigger events after A in the A data channel.

LED	MODE	TRIGGERING REQUIREMENTS
START A/ STOP B	SEQUENTIAL	Start data collection when A occurs; stop when B occurs (in the A data channel). If more than 250 words separate A and B, the most recent set of 250 are stored.
POS	TRIG MODE	Start data collection when all triggering conditions are met. Store the next 250 words.
NEG	TRIG MODE	Stop data collection when all triggering conditions are met. Store the previous 250 words.

4.2.2.2 STATUS LED'S

There are 3 additional LED's used to indicate the status of the Model 532.

LED	MODEL 532 STATUS	
OVERRIDE	AUTOMATIC MODE	Indicates that all front panel controls associated with data collection, plus certain other keyboard switches, are under external control.
ARMED	COLLECTION MODE	Indicates that the instrument is collecting data or ready to collect data. When ARMED LED is off, instrument is in DISPLAY mode.
PWR	ON	Indicates that the +5V output of the power supply is operating. (This indicator will be off if the fuse is blown.)

4.2.3 CONNECTORS

4.2.3.1 A & B DATA INPUT CONNECTORS

These connectors provide the interface for the data input probes. Each connector can accept 16-channels of data plus input clock and qualifying signals. Power and ground to the probes, plus a special user-defined signal called CNTRL, are also supplied through these connectors. Note that Model 50 and Model 51 probes can be used interchangeably with the A and B connectors.

CAUTION

ALWAYS INSERT THE KEYED DATA INPUT PROBE INTO THE A OR B CONNECTOR SUCH THAT THE "GROOVED" SIDE OF THE FLAT RIBBON CABLE FACES UP, ENSURING THAT THE PROBE LABEL IS ALSO FACING UP--OTHERWISE DAMAGE TO THE PROBE OR MODEL 532 MAY RESULT. FURTHERMORE, NEVER INSERT OR REMOVE PROBE CABLES WITH POWER APPLIED.

4.2.4 SWITCHES

4.2.4.1 A CLOCK EDGE SELECT (⌐ or ¬)

This is a 2-position switch which must be set to the active (rising or falling) edge of the incoming system clock. This clock edge selection relates to the clock used for both the A data channels and the B data channels if two-phase clocking is not employed. (See Section 4.2.4.2 below.)

4.2.4.2 B CLOCK EDGE SELECT (⌐ or ¬)

This is a 3-position switch whose upper and lower positions provide edge select functions identical to the A input clock. The third, or center position, A CLK, is used to tie the B clock to the A clock for 32-bit parallel clocking. In this mode, proper clock polarity for the entire 32-channels is selected by the A CLOCK EDGE SELECT switch.

4.2.4.3 A CLOCK QUALIFIER SELECT (1,X,0)

This 3-position switch is used in conjunction with an incoming signal from the system-under-test which gates the A data channel incoming clock. The logic level of the incoming qualifying signal required to enable the clock is selected as a 1 or 0, depending on the switch position. The center "X" position means "don't care" and functions to disable clock qualification requirements. Also note that 1, 0 refers to the logic notation used with the system-under-test, and not specific voltage levels. The TRUE/COMPLEMENT

switch on the probe inverts input data and qualifiers to accommodate both positive and negative true logic systems as follows:

PROBE SWITCH POSITION	LOGIC LEVEL	LOGIC SENSE
TRUE	HIGH	1
	LOW	0
COMPLEMENT	HIGH	0
	LOW	1

4.2.4.4 A TRIGGER QUALIFIER SELECT (1,X,0)

This 3-position switch is used in conjunction with an incoming signal from the system-under-test which gates the A data channel incoming trigger word. The logic level of the incoming qualifying signal required to enable the trigger word is selectable as 1 or 0, depending on the switch position. Note that the center position "X" means "don't care" and disables trigger qualification requirements. Here, again, the TRUE/COMPLEMENT switch on the probe has the affect described in the table in Section 4.2.4.3.

4.2.4.5 B CLOCK QUALIFIER SELECT (1,X,0)

This 3-position switch has the same functions for the B data channels as described in Section 4.2.4.3 for the A CLOCK QUALIFIER SELECT switch.

4.2.4.6 B TRIGGER QUALIFIER SELECT (1,X,0)

This 3-position switch has the same function for the B data channels as described in Section 4.2.4.4 for the A TRIGGER QUALIFIER SWITCH.

4.2.4.7 DELAY INC/DEC SELECT

This 3-position momentary switch (center off) controls the incrementing or decrementing of the value in the DELAY COUNT display. There are two modes of operation associated with each incrementing or decrementing action:

* Single-step: Momentarily moving the switch actuator from the center position for less than 1 second will change the delay value by 1 count.

* Sweep: Holding switch actuator off center for more than 1 second will cause the delay value to change rapidly.

4.2.4.8 CLOCK/OFF/TRIG SELECT

This 3-position switch selects the clock or trigger delay mode. The OFF position forces the delay value to 0000 without changing the displayed value in the DELAY COUNT readout and without using the DELAY INC/DEC SELECT switch or a keyboard command. In the CLOCK position, the delay count refers to input clocks. In the TRIG position, the delay value refers to trigger occurrences.

4.2.4.9 PAGE UP/ON SELECT

This 3-position momentary switch is used to manipulate the PAGE indicator. It provides the same single-step and sweep control functions described in Section 4.2.4.7 for the DELAY INC/DEC SELECT switch.

4.2.4.10 MAIN-M/A-AUX SELECT

This 3-position switch selects the contents of the main memory for display (MAIN), the contents of the auxiliary memory for display (AUX), or an alternating comparison between main and auxiliary memories (M/A).

4.2.4.11 A BIN/HEX/B BIN SELECT

This 3-position switch formats the contents of the selected memory in binary or hexadecimal. The A data channels (16-bits) can be displayed alone in binary (1's and 0's); the A and B data channels (32-bits) can be displayed together in hexadecimal; and the B data channels (16-bits) can be displayed alone in binary.

4.2.4.12 RESET/TRIG SELECT

This 3-position momentary switch functions as follows:

RESET position: Forces unit from DISPLAY mode into COLLECTION mode. The RESET switch also clears the OVERRIDE function when using the remote control modes and returns front panel control to the operator.

NOTE

RESET MUST BE ACTIVATED EACH TIME THE MODEL 532 IS POWERED UP TO DISABLE AUTOMATIC SELF TEST.

TRIG position: Forces the unit into the DISPLAY mode upon switch closure.

4.2.4.13 AUX. MEMORY SELECT

This 8-position rotary switch selects one of 8 auxiliary memory elements (1 RAM and 7 UV PROM SECTIONS) for READ or WRITE functions, depending on the keyboard command used.

4.2.4.14 DISPLAY TIME/HOLD

This potentiometer/switch combination controls the duration of time that each data collection is displayed. In the full CCW position, each data collection is displayed for approximately 20mS and then repeated. In the full CW position (just prior to the HOLD position), each data collection is displayed for approximately 10 seconds. In the HOLD position, a data collection is continuously displayed until the RESET switch described in Section 4.2.4.12 is activated.

NOTE

IF THE AUX. MEMORY BOARD IS USED WITH THE HOLD ≠ MODE, THE DISPLAY TIME/HOLD CONTROL FUNCTIONS ARE UNDER INTERNAL PROGRAM CONTROL. SEE SECTION 4.2.5.2.6.

4.2.5 KEYBOARD

The keyboard (Fig. 4.2-1) has two modes of operation: the CONTROL mode (CTL) and the DATA mode. The keyboard is normally in the CTL (shifted) mode, where the control functions labeled in black on the keys above the numbers and letters take precedence. There are 3 ways to "down shift" into the DATA mode:

1. Press SET A. The next entry is a 4-digit hex sequence (0-F,X) which establishes the value of the A trigger word.

2. Press SET B. The next entry is a 4-digit hex sequence (0-F,X) which establishes the value of the B trigger word.

3. Press SET DLY. The next entry is a 4-digit decimal sequence (0-9) which establishes the value of the delay. (Letter-keys are always ignored after the SET DLY key is pressed; only number-keys can create valid delay values.)

In order to return to the CTL mode, simply press the CTL key. From this point on, CONTROL-type changes in the operating mode of the instrument can be made without further pressing of the CTL key.

4.2.5.1 DATA MODE KEYS

The keys associated with the DATA mode are identified by white labels on the front panel and are listed below:

DATA MODE KEY	FUNCTION
0 - 9	Numeric portion of A or B trigger word or delay value or a data value targeted for an external µP's memory.*
A - F	Letter portion of A or B trigger word or data word targeted for an external µP's memory*
X	Sets any 4-bit group of the trigger word to "don't care."
READ	Permits the reading of the contents at the selected address of the external µP's memory.*
DEP	Write into selected address of external µP's memory.*
DEP+	Write into next address of external µP's memory.*

4.2.5.2 CONTROL MODE KEYS

These keys have seven functional groupings as described below.

*The external data entry function is for µP development applications when a personality probe is used with Model 532. (See Section 11.0.)

4.2.5.2.1 GROUP I - TRIGGER MODE KEYS: (A,B), (A,$\overline{B}$), (A=B, (A=$\overline{B}$), (A≠B), POS, NEG, START A/STOP B

These 8 keys correspond to the TRIGGER MODE LED's described in Section 4.2.2.1 which illuminate when the associated key is pressed.

4.2.5.2.2 GROUP II - DISPLAY CONTROL KEYS: WORD, TRIG, SIG

These 3 keys select which information is to be presented in the A and B DISPLAYS as described in Sections 4.2.1.1 and 4.2.1.2, respectively.

4.2.5.2.3 GROUP III - DATA ENTRY KEYS: SET A, SET B, SET DLY, READ, DEP, DEP+

These 6 keys shift the keyboard into the DATA mode for internal or external data entry as described in Section 4.2.5.1.

4.2.5.2.4 GROUP IV - AUXILIARY MEMORY CONTROL KEYS: SAVE, RECALL

The SAVE key initiates the transfer of data from the main memory into the selected auxiliary memory element. The data transferred includes the two signatures, the full 32 x 250 data collection, and the settings of the front panel used to obtain the data collection. If the RAM is selected, the transfer is straightforward; if one of the PROMS are selected, the appropriate PROGRAMMING VOLTAGE ENABLE switch on the Auxiliary Memory Board must first be activated and the PROM must be verified as blank by Model 532 software before data transfer can occur. Also, each 2716 PROM can contain two independent tests. The RECALL key places the front panel in the OVERRIDE mode and permits front panel settings stored in the selected auxiliary memory element to automatically control further data collections.

NOTE

DURING PROM PROGRAMMING, THE DELAY READOUT IS USED TO INCREMENT THE LOWER ADDRESS BYTE OF THE PROM TO INDICATE THAT PROGRAMMING IS OCCURRING. IF, FOR ANY REASON, A PROM CANNOT BE PROGRAMMED, AN EE (ERROR FLAG) INDICATION WILL APPEAR.

4.2.5.2.5 GROUP V - EXTERNAL INTERFACE CONTROL KEYS: REMOTE 1, REMOTE 2

These 2 keys activate external two-way communication interfaces. Remote 1 activates the RS-232C/TTY serial interface and Remote 2 activates the IEEE-488 interface. (See Appendices A.3 and A.4 for additional details.)

4.2.5.2.6 GROUP VI- BREAKPOINT KEYS: SET BP, HOLD ≠

These 2 keys activate breakpoint-type functions. The SET BP key is used with the personality probe in µP development applications of the Model 532 and provides a hardware-type breakpoint. (See Section 11.0.) The HOLD ≠ key provides a form of software breakpoint in the general-purpose analyzer mode and permits the Model 532 to trigger, collect, and hold when the data in the main memory are not equal to the data in the selected auxiliary memory element.

NOTE

THE HOLD ≠ MODE CAN ONLY BE USED WITH THE AUX. MEMORY OPTION. IN THIS MODE, THE DISPLAY TIME/HOLD CONTROL HAS NO AFFECT. UPON ENTERING THE HOLD ≠ MODE, THE ANALYZER WILL COLLECT DATA EACH TIME TRIGGERING CONDITIONS ARE SATISFIED AND CONTINUE COLLECTING UNTIL A DIFFERENCE IS DETECTED BETWEEN THE MAIN AND AUXILIARY MEMORY SIGNATURES. WHEN THIS DIFFERENCE OCCURS, ERRONEOUS DATA ARE HELD IN THE MAIN MEMORY. RESET MUST BE ACTIVATED TO CLEAR THE HOLD CONDITION.

4.2.5.2.7 GROUP VII - USER-DEFINED KEYS:

These 2 keys are spares which can be defined for custom applications by software resident in the User's Program Memory Board. See Section 6.15.

4.3 REAR PANEL

The rear panel is illustrated in Fig. 4.3-1.

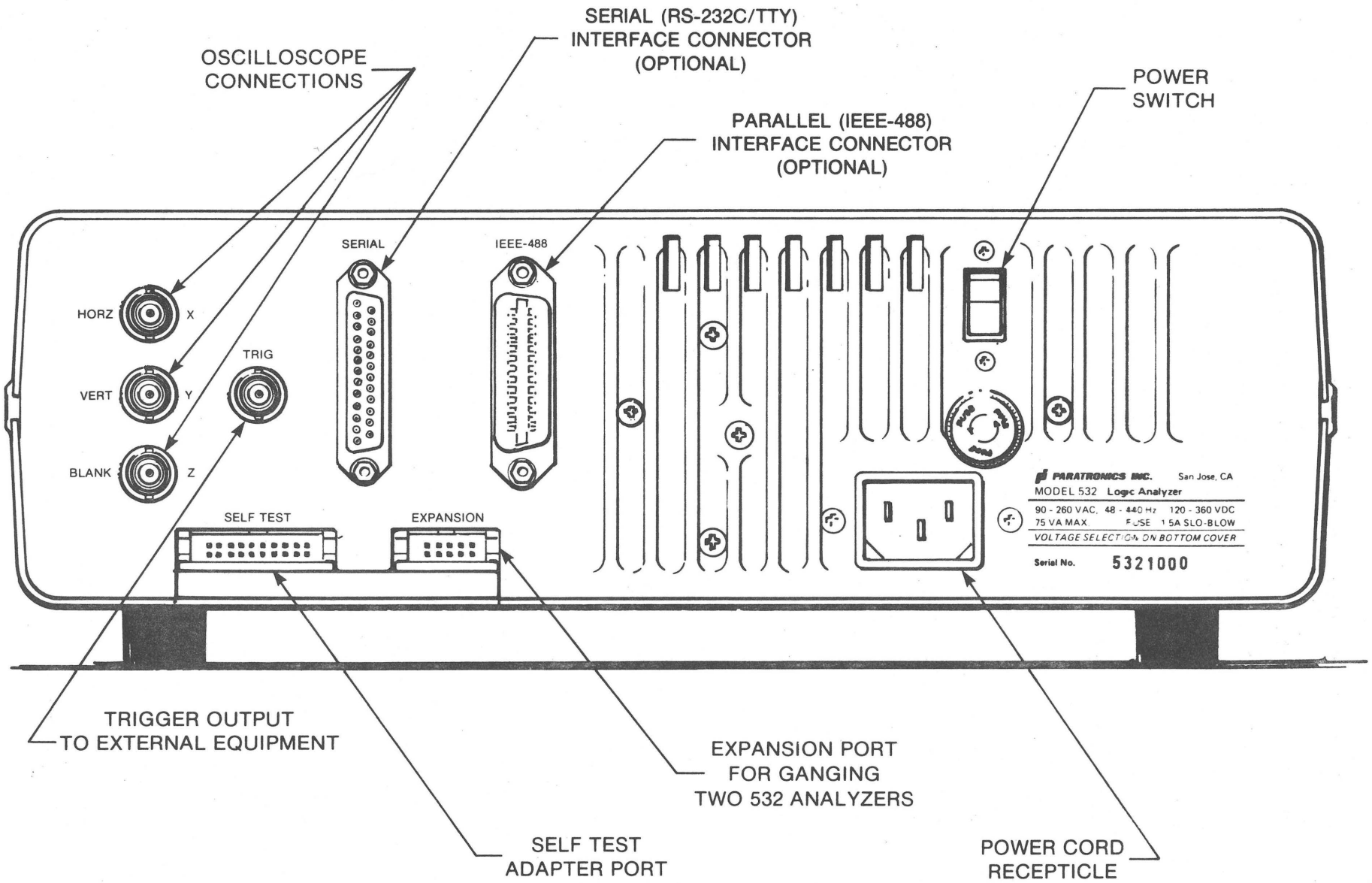


Fig. 4.3-1. The Model 532 rear panel.

4.3.1 SCOPE DISPLAY CONNECTORS

These are 3 BNC connectors at the left-hand-side of the rear panel which provides X (horizontal), Y (vertical), and Z (blanking) signals to an oscilloscope for writing the 16-word hex or binary truth table type of display.

4.3.2 TRIG CONNECTOR

This BNC connector provides a low-going TTL output pulse each time the Model 532 is triggered. The output pulse can be used as an external sync signal for scope triggering and analog troubleshooting, or as an input to a counter for computer performance monitoring. See Section 8.0 for TRIG output pulse timing information.

4.3.3 SELF-TEST CONNECTOR

This flat ribbon connector accepts the self-test adaptor. This permits the A or B data input probes to monitor the address bus of the Model 532's 8085 microprocessor, providing an individual end-to-end test of each data channel.

4.3.4 EXPANSION BUS

This flat ribbon compatible connector provides access to internal open collector RESET and TRIGGER BUS signals. These signals permit external control of the instrument as well as enabling multiple Model 532's to be ganged for analysis of more than 32 bits. (See Section 10.5.)

4.3.5 SERIAL CONNECTOR

This interface connector provides 2-way communication between the Model 532 and a compatible printer or video terminal.

4.3.6 IEEE-488 CONNECTOR

This interface connector provides 2-way communication between the Model 532 and a computer/controller.

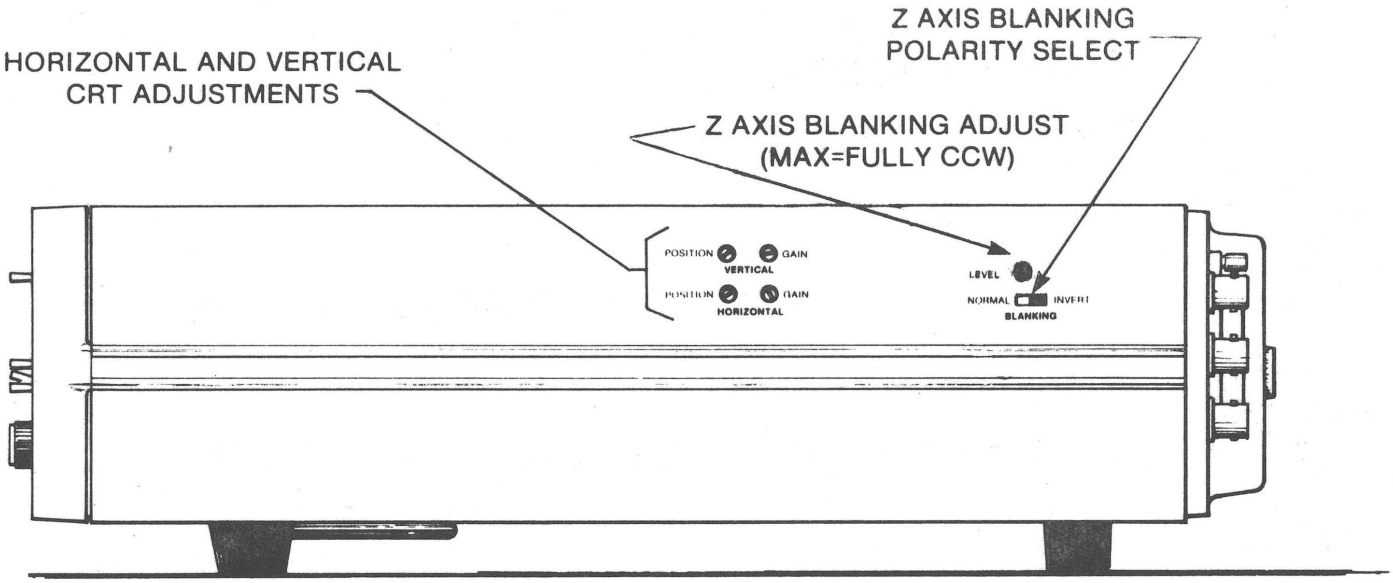


Fig. 4.4-1. Model 532 side view: Display controls.

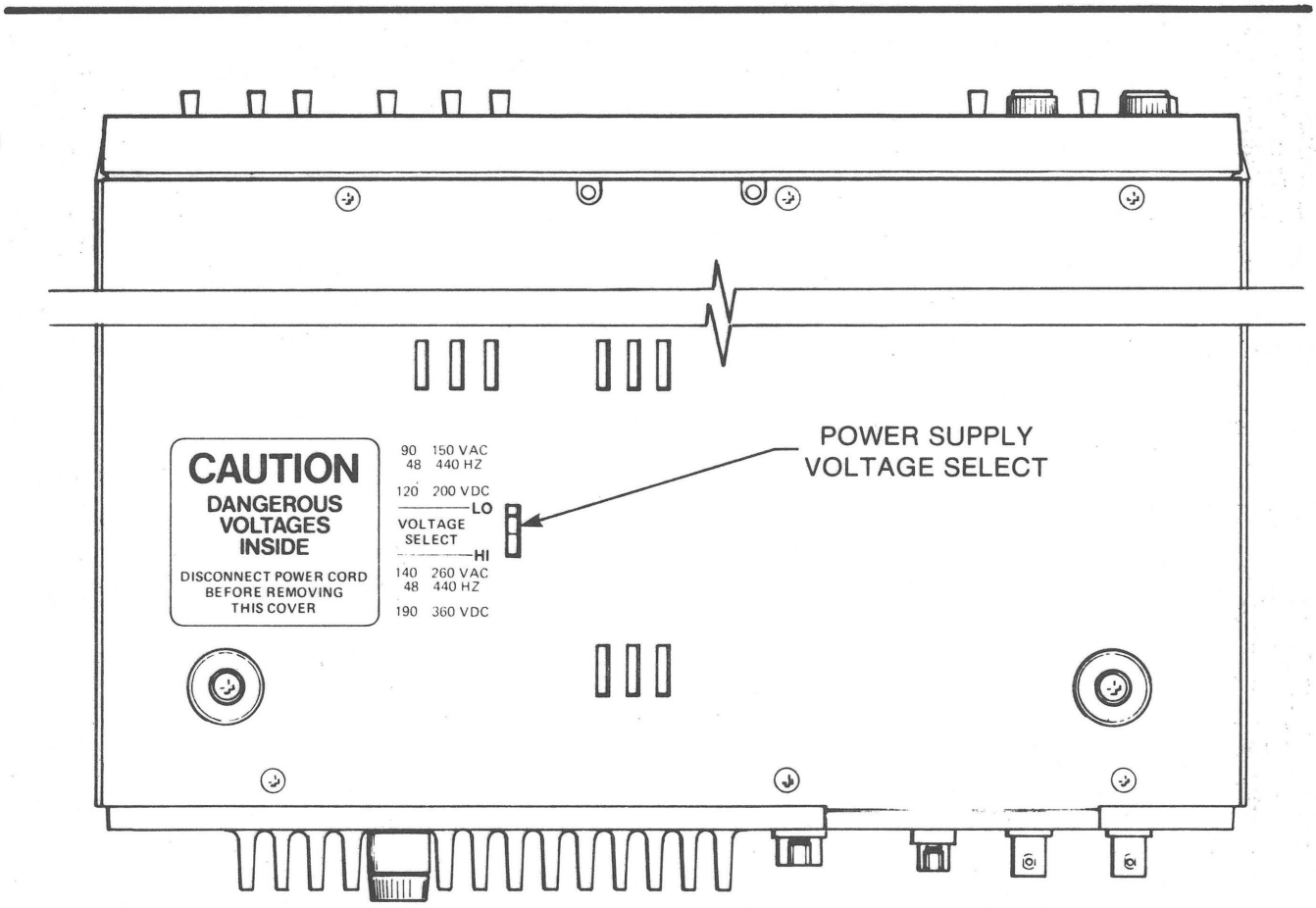


Fig. 4.4-2. Model 532 bottom view: AC power supply voltage select.

4.3.7 AC POWER RECEPTACLE

This receptacle accepts the 3-wire AC line cord.

4.3.8 FUSEHOLDER

The Model 532 requires a 1.5 AMP SLO-BLO type fuse.

4.3.9 ON/OFF SWITCH

This 2-position switch turns the AC power on and off.

4.3.10 SERIAL NO. LABEL

This label contains the identifying serial number plus fuse and AC power information.

4.4 MISCELLANEOUS EXTERNAL CONTROLS

The Model 532 has several miscellaneous controls located at the side and bottom of the instrument. (See Figs. 4.4.-1 and 4.4.-2.)

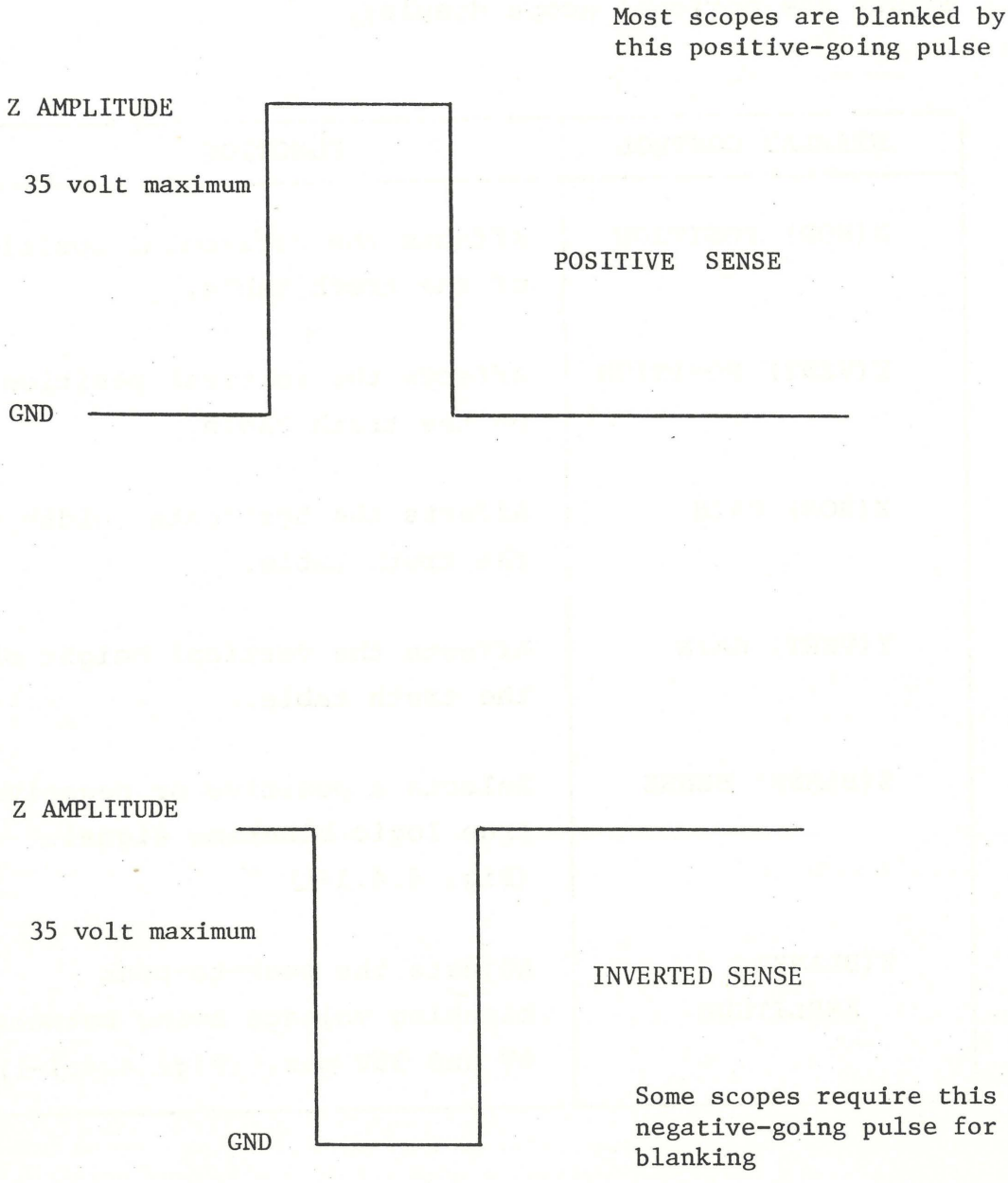
4.4.1 DISPLAY CONTROLS

These controls are shown in Fig. 4.4-1 and are used to adjust the optional scope display.

DISPLAY CONTROL	FUNCTION
X(HOR) POSITION	Affects the horizontal position of the truth table.
Y(VERT) POSITION	Affects the vertical position of the truth table.
X(HOR) GAIN	Affects the horizontal width of the truth table.
Y(VERT) GAIN	Affects the vertical height of the truth table.
Z(BLANK) SENSE	Selects a positive or negative true logic blanking signal. (Fig. 4.4.1-1)
Z(BLANK) AMPLITUDE	Adjusts the peak-to-peak blanking voltage swing between 0V and 35V max. (Fig. 4.4.1-1)

CAUTION

DO NOT EXCEED THE MAXIMUM BLANKING VOLTAGE ALLOWED BY THE MANUFACTURER OF YOUR SCOPE



NOTE: The Model 532 blanking output is not capable of going below the ground (or 0 volt) reference level

Fig. 4.4.1-1. Z-AXIS OUTPUT - Sense and amplitude definitions.

4.4.2 AC INPUT VOLTAGE SELECT

This 2-position switch is located at the bottom of the instrument, toward the rear. Access to the switch is through a cut-out in the bottom cover. (See Fig. 4.4-2.)

> **CAUTION**
>
> THIS SWITCH MUST BE SET TO THE POSITION CORRESPONDING TO THE AC LINE VOLTAGE USED BEFORE POWER IS TURNED ON. SEE SECTION 5.1.1.

The two AC voltage ranges available are:

90 - 150 VAC
140 - 240 VAC

The two DC voltage ranges available are:

120 - 200 VDC
190 - 350 VDC

4.5 MISCELLANEOUS INTERNAL CONTROLS

There are two types of controls accessible only by removing the top cover: User Controls and Calibration Controls. The User Controls include RS-232C/TTY, IEEE-488, and Auxiliary Memory Board controls and are described in Section 5.0. The Calibration Controls affect system timing and are set at the factory and THEY SHOULD NOT BE TAMPERED WITH. (See Maintenance Manual.)

5.0 INITIAL SETUP AND CHECKOUT

It is recommended that this section be reviewed completely before turning the unit on.

5.1 INITIAL SETUP

CAUTION

DO NOT INSERT THE 3-WIRE AC POWER CORD INTO THE REAR AC RECEPTACLE FOR THE FOLLOWING INITIAL STEPS.

Step 1. TOP COVER REMOVAL

Remove the top cover by loosening the captive fasteners and lifting and sliding the cover rear-wards.

Step 2. VISUAL INSPECTION

Check to see that all PC boards, cable assemblies, and IC's are securely seated in their sockets.

Note: Steps 3-6 below apply only if the unit is configured with one or more of the following optional PC boards:

* Auxiliary Memory Board
* User Program Memory Board
* Serial Interface Board
* IEEE-488 Interface Board

Step 3. AUXILIARY MEMORY ADJUSTMENT

If the Auxiliary Memory Board is present, check to see if the PROM PROGRAMMING VOLTAGE ENABLE switches are in the OFF position (DOWN).

Step 4. USER PROGRAM MEMORY ADJUSTMENT

Repeat Step 3 if the User Program Memory board is present.

Step 5. RS-232C/TTY ADJUSTMENT

If the RS-232 Serial Interface Board is present, set the BAUD RATE CONTROL switch in accordance with the instructions in Appendix A.3.

Step 6. IEEE-488 ADJUSTMENT

If the IEEE-488 Interface Board is present, set the TALKER and LISTENER ADDRESS switch in accordance with the instructions in the Appendix A.4.

Step 7. REPLACING TOP COVER

Replace the top cover by reversing the procedure in Step 1.

5.1.1 STAND-ALONE CHECK-OUT

In the following steps, a scope is not required. However, even if you plan to use the Model 532 with a scope, it is recommended that you perform the steps in this section as well as those in Section 5.2.1.

Step 1. VERIFICATION OF AC POWER OFF

Make sure the power ON/OFF switch at the rear of the unit is in the OFF position (top of Rocker depressed).

Step 2. SETTING THE AC INPUT VOLTAGE SELECT SWITCH

Set the AC INPUT VOLTAGE SELECT switch at the bottom of the unit to the proper position. Make certain the power cord is not plugged in. Insert a small screwdriver into the slot in the rear bottom cover and move the slide switch to the HI or LO position for the desired AC input voltage.

Step 3. SELF-TEST CONNECTIONS

Using the Model 53 SELF-TEST ADAPTOR, plug a Model 50 or Model 51 probe into the SELF-TEST PORT at the rear of the instrument. Plug the other end into the A data channel connector.

Step 4. A CHANNEL PROBE TRUE/COMPLEMENT SWITCH SETTING

Set the TRUE/COMPLEMENT switch on the A channel probe to TRUE.

Step 5. MODEL 51 PROBE THRESHOLD SETTING

If the Model 51 is used, set the TTL/VARIABLE threshold switch to TTL.

Step 6. INSERTION OF AC LINE CORD

Insert the 3-wire power cord to the mating receptacle at the rear of the unit.

WARNING

THE MODEL 532 IS EQUIPPED WITH A 3-WIRE SAFETY GROUND SYSTEM. DO NOT DEFEAT THIS SYSTEM BY BYPASSING THE SAFETY GROUND; OTHERWISE, AN INTERNAL FAILURE COULD CAUSE THE CHASSIS TO BECOME "HOT," POSSIBLY RESULTING IN SERIOUS INJURY OR DEATH TO THE OPERATOR.

Step 7. SETTING UP FRONT PANEL CONTROLS

The front panel is shown again in Fig. 5.1.1-1 for convenience. Set up the front panel switches as follows:

FRONT PANEL SWITCH	SETTING
A CLOCK EDGE SELECT	RISING EDGE (⌐)
B CLOCK EDGE SELECT	CENTER POSITION
A CLOCK QUALIFIER SELECT	" "
A TRIGGER QUALIFIER SELECT	" "
B CLOCK QUALIFIER SELECT	" "
B TRIGGER QUALIFIER SELECT	" "
CLOCK/OFF/TRIG SELECT	" "
A BIN/HEX/B BIN SELECT	" "
MAIN-M/A-AUX SELECT	MAIN
AUX. MEM. SELECT	RAM
DISPLAY TIME/HOLD	HOLD (FULLY CW)

CAUTION

NEVER APPLY POWER TO THE INSTRUMENT UNLESS YOU ARE CERTAIN THAT THE AC INPUT VOLTAGE SELECT SWITCH IS SET TO THE PROPER POSITION.

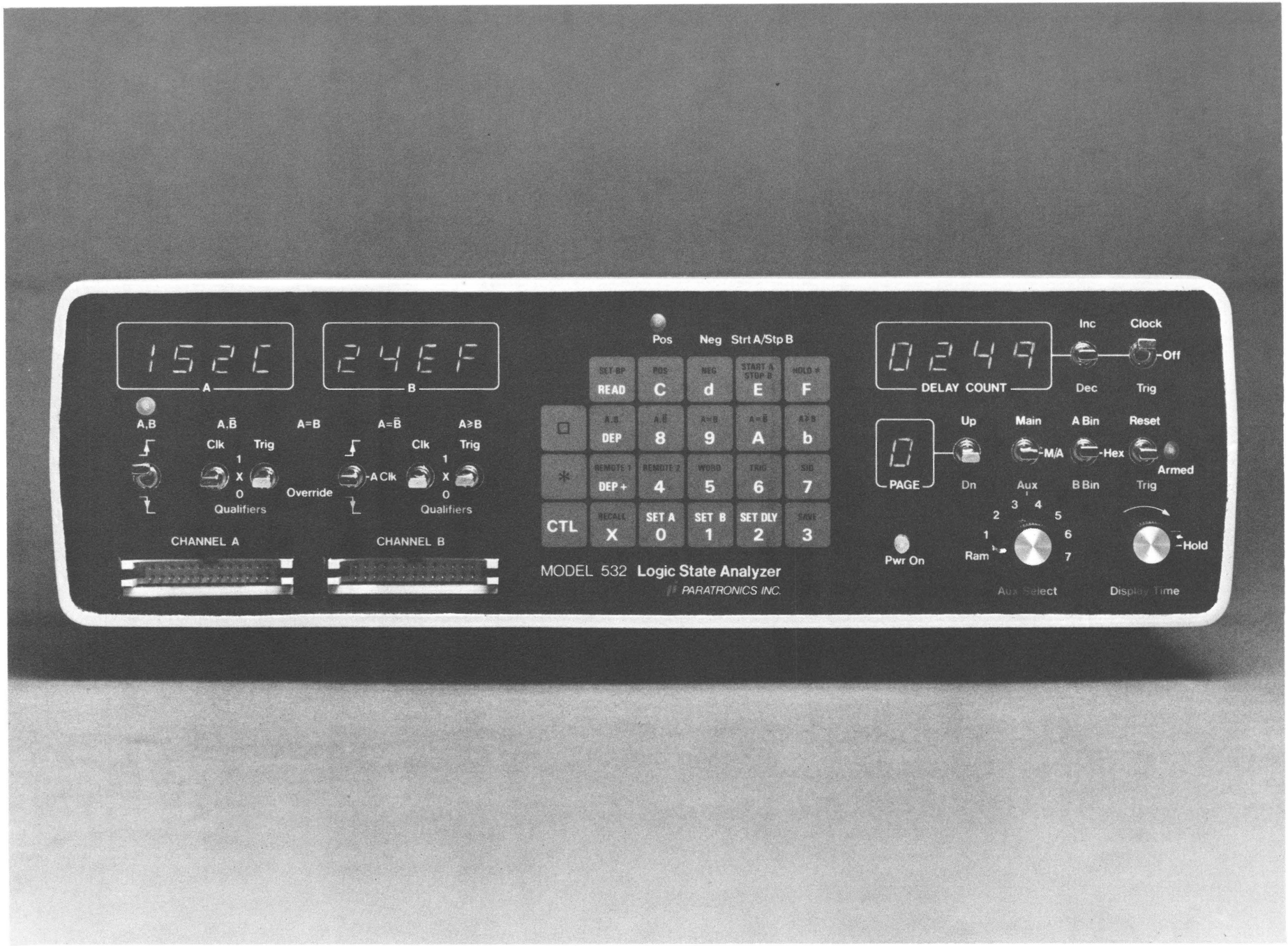


Fig. 5.1.1-1. Model 532 front panel.

Step 8. TURNING POWER ON

Turn the unit on by switching the power ON/OFF switch at the rear of the unit to ON (bottom of rocker depressed).

Step 9. VERIFICATION OF LED INDICATORS

After approximately a one second reset period, verify that the front panel LED indicators display the following information:

READOUT	INDICATION
PWR	ON
A DISPLAY	SELF-TEST SIGNATURE (A)
B DISPLAY	SELF-TEST SIGNATURE (B)
DELAY	0000
PAGE	0
(A,B)	ON
POS	ON
OVERRIDE	ON

NOTE

FOR THIS SELF-TEST SET-UP, THE PROBE IS MONITORING THE ADDRESS BUS OF THE INTERNAL MICROPROCESSOR. THE ANALYZER IS PROGRAMMED TO AUTOMATICALLY ENTER THE SELF-TEST ROUTINE UPON POWER UP, REGARDLESS OF THE SETTINGS OF THE FRONT PANEL CONTROLS. THEREFORE, ANY TIME MODEL 532 OPERATION IS IN QUESTION, CONNECT THE UNIT FOR SELF-TEST, TURN POWER ON, AND CHECK THE SIGNATURES. HOWEVER, UNLESS THE SWITCHES ARE SET AS DESCRIBED IN STEP 7, SUBSEQUENT STEPS IN THIS SECTION CANNOT BE PERFORMED.

Step 10. TROUBLESHOOTING

If the front panel LED's are not displaying the above information, turn the unit off and review the procedure in Steps 7 and 8. If you are still having difficulty, refer to the Maintenance Manual.

NOTE

IF ALL THE DISPLAYS ARE BLANK, TURN THE UNIT OFF, REMOVE THE AC POWER CORD AND CHECK THE FUSE. ALSO CHECK TO SEE THAT THE AC POWER SWITCH AT THE BOTTOM OF THE UNIT IS SET TO THE PROPER AC LINE VOLTAGE.

Step 11. RESETTING UNIT

Reset the unit using the RESET/TRIG switch to gain control of the front panel. Note that the OVERRIDE LED goes out.

Step 12. REVIEW SECTIONS 4.2.2.1 and 4.2.5

You are ready to exercise the keyboard. Before continuing, it is a good idea to review Sections 4.2.2.1 and 4.2.5 to make sure that keyboard modes and responses are understood.

NOTE

IN THE STAND-ALONE MODE, THE PAGE DISPLAY AND THE ASSOCIATED UP/DN CONTROL ARE NOT USED. THE PAGE DISPLAY IDENTIFIES THE PARTICULAR 16-WORD TRUTH TABLE BEING ANALYZED WHEN A CRT IS USED WITH THE ANALYZER.

Step 13. ENTERING THE TRIGGER MODE

Press the TRIG key to enter the TRIGGER mode. The A display should show 0040 (the starting address of the self-test program); and the B display should be blank (don't care).

Step 14. CHANGING THE DISPLAY TIME

INITIAL CONDITIONS: (A,B), TRIG, POS; A=0040, B=XXXX, DLY=0000.

Rotate the DISPLAY TIME/HOLD switch CCW until the displays blink about once every second.

Step 15. CHANGING THE A TRIGGER WORD

INITIAL CONDITIONS: (A,B), POS; A=0040, B=XXXX, DLY=0000

Press the SET A key followed by the number keys: 0-0-4-2. The A DISPLAY should change from 0040 to 0042, indicating that the Model 532 will collect data starting from address 0042. If an error is made in entering a value, simply continue until the display shows the desired value. At any time, the value displayed is the current trigger word.

Step 16. CHANGING THE B TRIGGER WORD

INITIAL CONDITIONS: (A,B), TRIG, POS; A=0042, B=XXXX, DLY=0000

Press CTL, then the SET B key followed by F-F-F-F. The B DISPLAY should now read FFFF. Since the instrument automatically comes up in the (A,B) or parallel triggering mode during self-test, you have satisfied this mode by setting up a valid 32-bit trigger word as follows: 0042 FFFF. (Note that in the self-test mode, the B data channels are always satisfied by a B trigger word value of FFFF since there is no probe connected to the B data input and, therefore, the input logic assumes the default state of all "1's.")

Step 17. EXPERIMENTING WITH VALID AND INVALID TRIGGER WORDS

INITIAL CONDITIONS: (A,B), TRIG, POS; A=0042, B=FFFF, DLY=0000

Observe the effect of keying-in different trigger words in the A and B displays while watching the ARM

LED. When this LED is off, the trigger word is valid (i.e., the value exists at the input); when it is on, the trigger word is invalid. (Note: if a CRT display were connected, a valid trigger word would produce a 16-word truth table; otherwise the truth table would not be evident.)

Step 18. AC POWER OFF

Turn AC-power off.

Step 19. B CHANNEL PROBE TRUE/COMPLEMENT SWITCH SETTING

Make sure the TRUE/COMPLEMENT switch on the B channel Model 50 probe is set to the TRUE position. (If the Model 51 probe is used, make sure the TTL/VARIABLE threshold switch is set to TTL and the TRUE/COMPLEMENT switch is set to COMPLEMENT.)

Step 20. B CHANNEL PROBE CONNECTION

Carefully insert the second Model 50 or Model 51 probe into the B channel input connector. Do not connect the probe to any logic circuit.

CAUTION

MAKE SURE THAT THE PROBE IS INSERTED WITH THE "GROOVED" SIDE OF THE RIBBON UP; OTHERWISE SERIOUS DAMAGE TO THE INSTRUMENT OR PROBE ITSELF MAY RESULT WHEN THE UNIT IS TURNED ON.

Step 21. AC POWER BACK ON

Switch the Model 532 power on, press the RESET switch and then press the TRIG key.

Step 22. SETTING UP VALID A AND B TRIGGERING WORDS

With the A display at 0040, set the B display to FFFF. The ARM LED should be off, indicating proper triggering.

Step 23. GENERATING AN INVALID B TRIGGER WORD

INITIAL CONDITIONS: (A,B), TRIG, POS; A = 0040, B = FFFF, DLY = 0000

Switch the TRUE/COMPLEMENT switch on the B channel probe to the other position, forcing the input data to invert. Note that the ARM LED is on, indicating an invalid trigger word. Now change the B DISPLAY to read 0000 by pressing SET B and 0-0-0-0. Note that the ARM LED goes off, indicating that the Model 532 is now triggering.

Step 24. TESTING THE (A,$\overline{B}$) TRIGGERING MODE

INITIAL CONDITIONS: (A,B), TRIG, POS; A = 0040, B = 0000, DLY = 0000

Press the CTL key to return the keyboard to the CONTROL mode. Then press the (A,$\overline{B}$) key. Note that the ARM LED comes on again. Now switch the B channel probe TRUE/COMPLEMENT switch back to the original position. The ARM LED should go off, indicating that the analyzer is triggering on the occurrence of A and not the occurrence of B. Next, press SET B and F-F-F-F and note that the ARM LED comes on again. Finally, press the E key and note that the B DISPLAY changes to FFFE accordingly, and that the Model 532 again triggers.

Step 25. TESTING THE (A=B) TRIGGERING MODE

INITIAL CONDITIONS: (A,$\overline{B}$), TRIG, POS; A = 0040, B = FFFE, DLY = 0000

Press the CTL key to return the analyzer to the CONTROL mode. Press the (A=B) key: the ARM LED should go on. Press SET B and 0-0-4-2. Then move the CLOCK/OFF/TRIG switch to the CLOCK position. Increment the delay INC/DEC switch by 3 counts so that a delay value of 0003 appears in the

DELAY COUNT readout. Note that the ARM LED goes out since B follows A by 3 delay units. (Three program steps separate the A and B addresses.) Finally, increment the delay value to 0004 and and the ARM LED will come back on.

Step 26. TESTING THE (A=$\overline{B}$) TRIGGERING MODE

INITIAL CONDITIONS: (A=B), TRIG, POS; A = 0040, B = 0042, DLY = 0004

Press the CTL key and then the (A=$\overline{B}$) key: the ARM LED will go off. Decrement the value in the DELAY CONTROL to read 0003. Now the ARM LED will go on, indicating that the correct value for B is occurring at a delay of 0003. Decrement the delay value to 0000; the ARM LED will again go off.

> NOTE
>
> ALL 21 POSSIBLE TRIGGERING MODES AND RESPONSES CANNOT BE TREATED IN THIS INITIAL CHECKOUT SECTION. REFER TO SECTION 8.0 FOR ADDITIONAL INFORMATION BEYOND THE BASIC TRIGGERING INFORMATION COVERED HERE.

Step 27. RETURN TO PARALLEL TRIGGERING MODE

INITIAL CONDITIONS: (A=$\overline{B}$), POS, A = 0040, B = 0042, DLY = 0000

Press the CTL key followed by the (A,B) key. Press SET B and F-F-F-F. The B channel probe TRUE/COMPLEMENT switch should be in the TRUE position for the Model 50; or the COMPLEMENT position for the Model 51 probe. Verify that the ARM LED is off to indicate that the analyzer is triggering. Make sure the CLOCK/OFF/TRIG switch is in the CLOCK position for the next step.

Step 28. USING THE WORD DISPLAY, POS MODE, CLOCK DELAY=ZERO

INITIAL CONDITIONS: (A,B), CLOCK, POS; A=0040, B=FFFF, DLY=0000

Rotate the DISPLAY TIME/HOLD control to the HOLD position (full CW). Press RESET to obtain a new collection. Then press the CTL key followed by the WORD key to place the analyzer in the WORD DISPLAY mode. Check the DELAY COUNT readout to ensure that it is displaying 0000. (Remember that in the WORD mode, the DELAY COUNT readout functions as a word locator and may have an initial value which is non-zero. If this is the case, press SET DLY followed by 0-0-0-0.)

In the WORD mode, the A and B display should still read 0040 and FFFF since the trigger word and WORD 0 in the data memory are the same in this case. Now increment the DELAY INC/DEC switch so that the delay value reads 0001. The A and B displays should now read 0041 and FFFF, respectively, which is WORD 1 in the data memory. Increment the delay value to 0002 and observe WORD 2, which is made up of a special 4-digit number in the A display and FFFF in the B display. This special number in the A display is the revision number of the internal 8085 operating software. It only appears in the self-test configuration. Next decrement the delay value back towards 0000 and note that further decrementing below 0000 is inhibited. This is because, in the POS mode, WORD 0 is the first word collected: there are no prior words in the data memory.

In order to examine the last word collected, press SET DLY followed by 0-2-4-9. At this point, the A and B displays will show WORD 249, or the 250th word collected, counting WORD 0. Increment the delay value by 1 count and note that the DELAY COUNT readout automatically "rolls over" to 0000. (Note that for software implementation reasons, it will not roll back to 0249 from 0000--this is normal.)

Next, key in any 4-digit delay value greater than 0249 using the keyboard; you'll find that the analyzer rejects delay values in the WORD mode greater than 0249 and sets the DELAY COUNT readout automatically back to 0000.

Fig. 5.1.1-2 illustrates the arrangement of data words in the analyzer's memory using the positive (post-trigger) collection mode. Finish this step with a word locator value of 0000.

Step 29. USING THE WORD DISPLAY, POS MODE, NON-ZERO CLOCK DELAY

INITIAL CONDITIONS: (A,B), WORD, POS; A = 0040, B = FFFF, DLY = 0000

Return to the TRIG mode by pressing CTL followed by the TRIG key. Increment the delay value to 0003. Then press RESET to obtain a new data collection beginning 3 clock delays after 0040, FFFF.

Enter the WORD mode by pressing the WORD key. Note that the DELAY COUNT readout indicates 0000 since this was the last word locator value used in Step 30.

Note also that the first word in the data memory (WORD 0) is (0042,FFFF)--or the value of the 8085 address bus which is precisely 3 clock delays after the trigger word (0040,FFFF).

Step 30. USING THE WORD DISPLAY, NEG MODE, CLOCK DELAY = ZERO

INITIAL CONDITIONS: (A,B), WORD, POS; A = 0042, B = FFFF, DLY = 0000

Press the TRIG key and decrement the delay value to 0000. Then press NEG to enter the pre-trigger data collection mode. Next, press RESET to obtain a

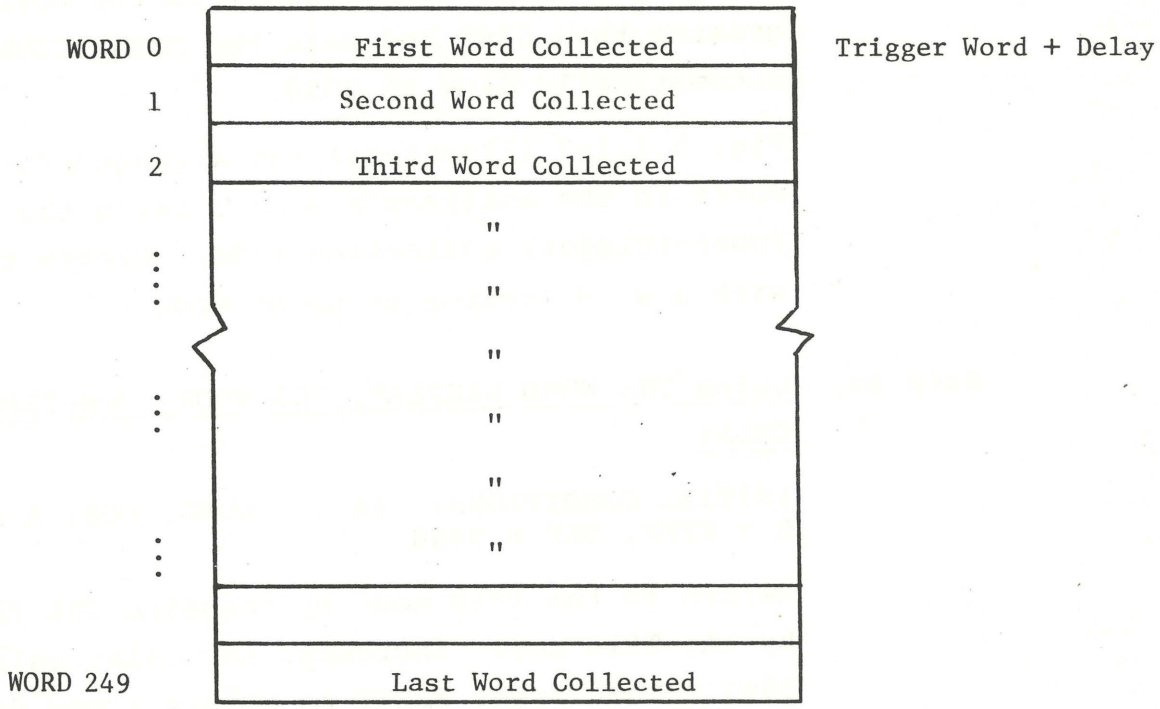


Fig. 5.1.1-2. Arrangement of data words in memory using the WORD mode with positive (post-trigger) collection.

new collection. Enter the WORD mode by pressing the WORD key and observe 0040 and FFFF again displayed. However, in this case, these values represent the last word collected. Press SET DLY followed by 0-2-4-9 to observe the first word collected. Increment the delay value by 1 and note that the word locator again "rolls over" to 0000 and cannot be decremented below this value.

Fig. 5.1.1.-3 illustrates the arrangement of data words in the analyzer's memory using the negative (pre-trigger) collection mode. Finish this step with a delay value of 0000.

Step 31. USING THE WORD DISPLAY, NEG MODE, NON-ZERO CLOCK DELAY

INITIAL CONDITIONS: (A,B), WORD, NEG; A = 0040, B = FFFF, DLY = 0000

Press CTL to return to the CONTROL mode followed by TRIG. Increment the clock delay value to 0003 and press RESET to obtain a new collection. Return to the WORD mode with a delay value of 0000 and observe that the last word in the data memory is (0042,FFFF)--which is the address value of the 8085 occurring precisely 3 clock pulses after the trigger (0040, FFFF).

Step 32. USING THE WORD DISPLAY AND THE START A/STOP B TRIGGER MODE

INITIAL CONDITIONS: (A,B), WORD, NEG; A=0040, B=FFFF, DLY=0000

Press START A/STOP B and TRIG. Press SET B followed by 0-0-4-2. Decrement the clock delay value to 0000. Press RESET for a new data collection. In this mode, the analyzer starts collecting data when 0040 occurs and stops when 0042 occurs. At this point, the data memory contains only 4 words: (0040,FFFF), (0041,FFFF),

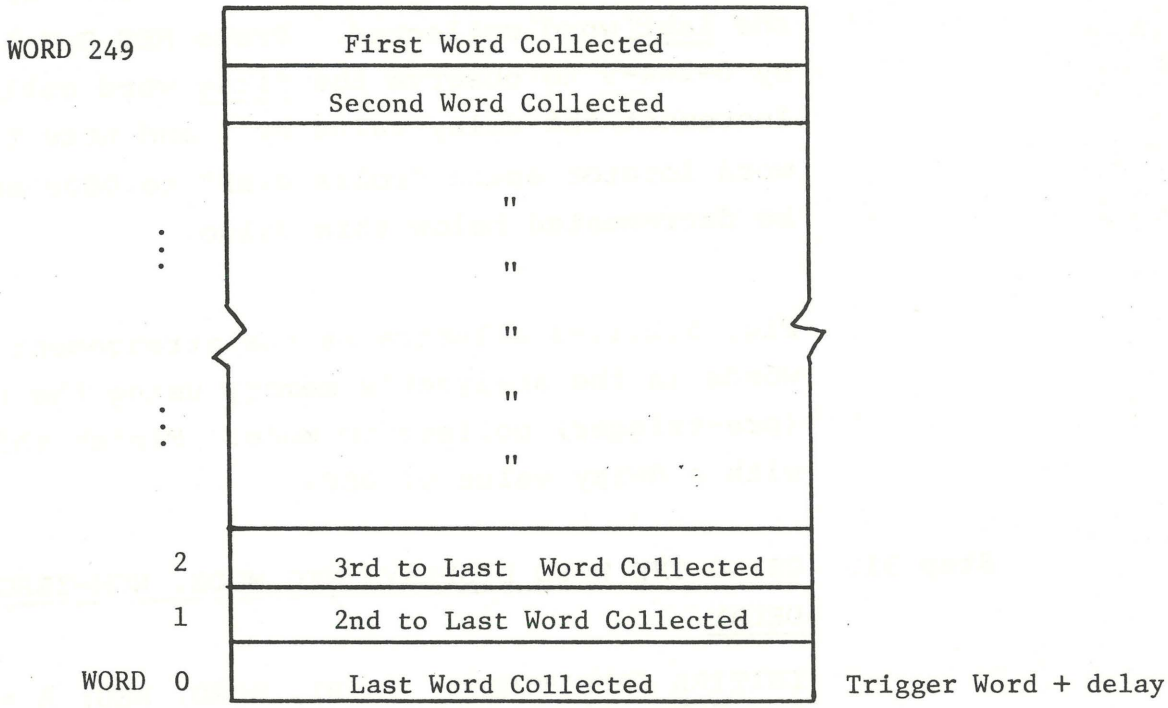


Fig. 5.1.1.-3. Arrangement of data words in memory using WORD mode with negative (pre-trigger) collection.

(software revision no., FFFF), and (0042,FFFF).

In order to check memory contents and boundaries, press CTL and WORD to enter the WORD mode. Then increment the word locator from 0000 to 0003. Note the memory contents and note that the DELAY COUNT readout rolls over to 0000 after reaching the memory boundary of 0003. Finish with a word locator value of 0000 in the DELAY COUNT readout.

NOTE

WHEN YOU ENTER THE START A/STOP B MODE, THE MODEL 532 SOFTWARE AUTOMATICALLY PLACES THE ANALYZER IN THE POS MODE SINCE THE NEG MODE DOES NOT MAKE SENSE HERE. IN FACT, THE NEG MODE IS INHIBITED BY THE SOFTWARE. THUS, THE START A/STOP B MODE CANNOT BE CHANGED BY PRESSING THE POS OR NEG KEYS; IT CAN ONLY BE CHANGED IF ANOTHER TRIGGER MODE (SUCH AS (A,B), (A=B), ETC.) IS SELECTED.

Step 33. TESTING THE TRIG DELAY

INITIAL CONDITIONS: START A/STOP B, WORD, A = 0040, B = 0042, DLY = 0000.

Press CTL, (A,B), TRIG, SET B, X-X-X-X (don't care), CTL and SET DLY followed by 0-1-2-5. Change the CLOCK/OFF/TRIG switch to the TRIG position. For this setting, the delay value refers to the number of times the trigger word must occur before the analyzer will trigger. Press RESET: after approximately 4.0 seconds, the ARM LED will go off, indicating the 125 trigger words have occurred. Return the CLOCK/OFF/TRIG switch to the CLOCK position and set the DISPLAY/TIME control for approximately 1 or 2 collections/seconds. Finish this step with a delay value of 0000.

Step 34. TESTING THE A CLOCK QUALIFIER

INITIAL CONDITIONS: (A,B), TRIG, POS; A = 0040, B = XXXX, DLY = 0000

Press CTL and SET A followed by 7-E-7-E. Move the A CLOCK QUALIFIER switch from X to 1. This action forces the analyzer's input circuits to accept data only when the trigger word occurs and the associated self-test status bit is high. (During self-test, the status bit used is high when an internal I/O operation is occurring and low when a memory reference operation is occurring.) The ARM light should go out when the I/O operation at A = 7E7E occurs. Press CTL and activate the WORD mode. Increment the INC/DEC switch and observe that all A values have identical upper and lower bytes. This is the I/O Address Mirror of the 8085 and indicates that the analyzer's memory now contains all I/O operations. Return the A CLOCK QUALIFIER switch back to X. Also, press the TRIG key and return to a delay value of 0000.

Step 35. TESTING THE A TRIGGER QUALIFIER

INITIAL CONDITIONS: (A,B), TRIG, POS; A = 7E7E, B = XXXX, DLY = 0000

Press SET A followed by 0-0-4-0. Move the A TRIG QUALIFIER switch from X to 0. This action forces the analyzer's input circuits to begin collecting data when the trigger word occurs and the self-test trigger qualifier line is low. In this case, the qualifier line used is the internal READ/WRITE line which is 0 when a READ operation occurs and 1 when a WRITE occurs. The ARM light should go off indicating that a read operation occurred at location 0040. Using this qualifying sigal, the analyzer triggers as soon as the first READ operation occurs and collects the next 250 words without

further qualification. (Note that the 1 position causes the ARMED LED to come on.) Return the A TRIG QUALIFIER switch to the X position.

Note: Skip Steps 36 and 37 if your Model 532 is not equipped with the Auxiliary Memory Board option.

Step 36. TESTING THE AUXILIARY MEMORY BOARD USING RAM

INITIAL CONDITIONS: (A,B), TRIG, POS; A=0040, B=XXXX, DLY=0000

With the DISPLAY TIME/HOLD control set to the left (approx. 10:00), press CTL followed by SET B and 0-0-4-2. Then press CTL and START A/STOP B. Press RESET and activate the WORD mode and view the following 4 words in the data memory: WORD 0 (0040,FFFF); WORD 1 (0041,FFFF); WORD 2 (software rev. no., FFFF); and WORD 3 (0042, FFFF). Finish with WORD 2 (software rev. no., FFFF) in the A and B displays. This line of data represents an 8085 I/O address which is used to identify the Model 532's current operating software. Now move the A CLOCK QUALIFIER switch between X and 0 and note that this line can be deleted and thus replaced by the next word, (0042,FFFF). This is because the A clock qualifier line, for the purpose of self-test, is connected to the 8085 I/O status line. This line is a logic 1 whenever an I/O operation occurs. Therefore, by setting the A CLOCK QUALIFIER switch to 0, I/O operations are "qualified out." Now move this switch back to X to again view the I/O operation.

Select the RAM position of the AUX. MEMORY rotary switch. Press the SAVE key to store the 4 words, the signatures, and the front panel settings. (Of course, for other examples, up to 250 words can be stored in each auxiliary memory element.) Move the MAIN-M/A-AUX switch to the M/A position to compare the data in the main and auxiliary memories and note that they are the same. With this switch in the M/A position, again delete the I/O operation by

moving the A CLOCK QUALIFIER switch to 0. Notice that the A display alternates between the software rev. no. (WORD 2) and 0042 (WORD 3), while the B display remains static for this example. Now press SIG and observe the alternating signatures. If a large number of words were collected, the flashing signatures would be used to identify main and auxiliary memory differences without examining each line. Press WORD to return to the WORD mode.

Next move the MAIN-M/A-AUX switch to MAIN to view a steady 0042 (new WORD 2) and then to AUX to view a steady software rev. no. (old WORD 2). Finish with the switch back in the M/A position.

Now press SET A followed by 1-2-3-4 to enter a non-valid trigger word. This will cause the A and B displays to go blank and the ARMED LED to turn on. Press CTL and TRIG to see the A and B trigger words: (1234, 0042). Press (A,B) to change modes. Then press SET B followed by 5-6-7-8 and CTL and SET DLY followed by 9-9-9-9. Obviously, the triggering mode has been drastically changed. In order to automatically reproduce the stored test, simply press CTL followed by RECALL. Note that the A display shows 0040, the B display shows 0042, the delay count shows 0000, and the mode is back to START A/STOP B. Also note that the OVERRIDE LED is on, indicating that all front panel functions affecting triggering are inhibited and data collected remains under control of the internal operating program. In order to illustrate this, press SET A followed by 1-2-3-4. Then press CTL and (A,B) to try to change the mode from START A/STOP B to (A,B). Note that there is no affect. Press the WORD key and again observe the software rev. no. in the A display. Also note that the A CLOCK QUALIFIER switch has no affect in the 0, X, or 1 position since the original stored test in the RAM was accomplished with this switch in the X position and the

current automatic data collection is on this basis. Place this switch in the 0 position, and with the MAIN-M/A-AUX switch in the M/A position, press RESET to regain front panel control. Again note the flashing data in the A display. Rotate the DISPLAY TIME/HOLD control CCW and observe that the collection and comparison function can be increased. Move the A CLOCK QUALIFIER switch to X to view a steady display of WORD 2 and press the HOLD ≠ key. Now move the A CLOCK QUALIFIER switch to 0 and back to X. Note that the A display continues to flash, even with the switch in the X position. Also note that rotation of the DISPLAY TIME/HOLD control has no affect of the flashing rate. Both of these differences are functions of the HOLD ≠ mode which causes the analyzer to continuously hold and compare the first real-time data collection which differed from the data in the RAM. Thus, the HOLD ≠ mode, though software, automatically forces the DISPLAY TIME/HOLD control to the HOLD position so as to prevent the inadvertent missing of a transient event (which is the primary function of this mode).

In order to escape from the HOLD ≠ mode, press the RESET switch. Finish this step by returning to the TRIG mode, placing the A CLOCK QUALIFIER in the X position, selecting the MAIN memory for display, and adjusting the DISPLAY TIME/HOLD control for about 1 collection/second (approx. 10:00).

Step 37. TESTING THE AUXILIARY MEMORY BOARD USING PROM

INITIAL CONDITIONS: START A/STOP B, TRIG; A=0040, B=0042, DLY=0000

If it is desired to retain a particular test, one of the seven PROM elements may be selected. The procedure and functions described in Step 36 for the RAM are identical for the PROM, with the following exceptions:

1. As a precautionary feature, each PROM must be activated by the associated PROGRAMMING VOLTAGE ENABLE switch before the SAVE (programming) function can occur. (See Fig. 5.1.1.-4.) Also, before the RECALL function can be used, the associated programming switch must be deactivated.

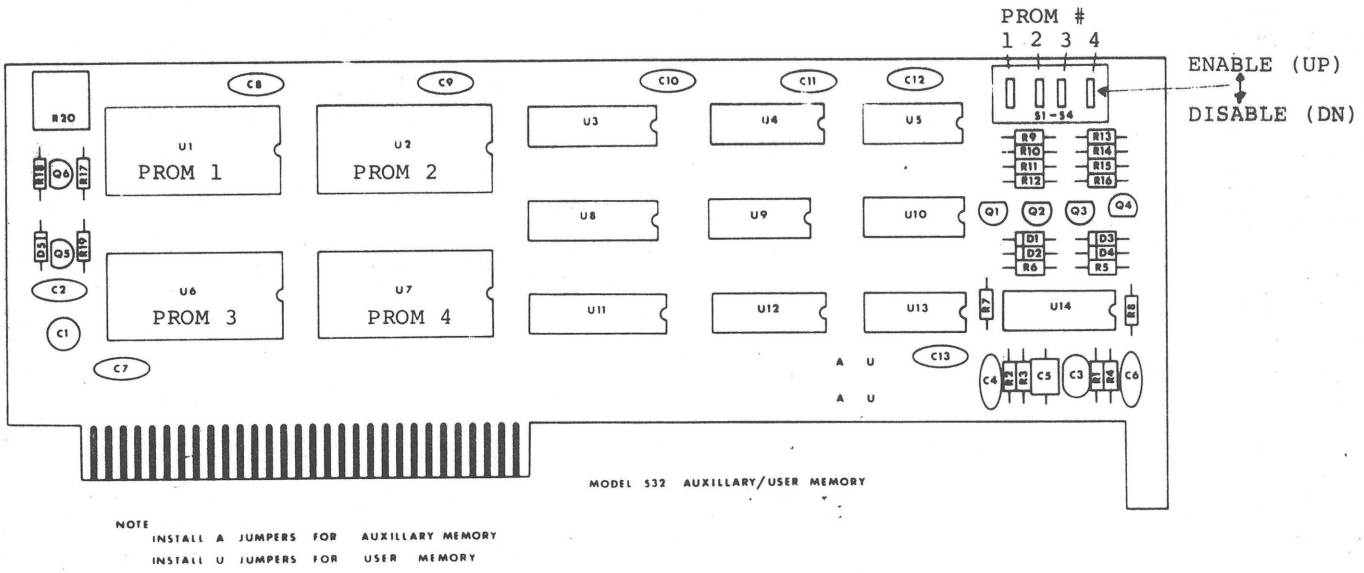
2. During programming, the DELAY COUNT readout displays the incrementing of the lower 8 bits of the address of the particular PROM being programmed. (A 250-word data transfer takes about one minute.) However, if the PROM enable switch is in the wrong position, or the PROM has been programmed already, or the PROM socket is empty, or if the PROM is defective, an EE (error) indication will appear in the readout.

NOTE

THE 4 UV PROMS NORMALLY USED IN THE AUXILIARY MEMORY BOARD ARE INTEL 2716'S. EACH PROM CAN CONTAIN 2 INDEPENDENT AND COMPLETE TESTS; HOWEVER, AN EIGHTH TEST, WHICH NORMALLY WOULD RESIDE IN THE SECOND HALF OF PROM 4, IS PRESENTLY NOT USED. NOTE THAT THE AUXILIARY MEMORY BOARD WILL ALSO STORE TESTS IN INTEL 2758 UV PROMS. SEE FIG. 5.1.1-4 FOR DETAILS.

NOTE

2716 PROMS MAY BE ERASED USING A UV LIGHT DESIGNED FOR THAT PURPOSE. THE SPECIFIC PROM REQUIRING ERASURE MUST BE REMOVED FROM THE AUXILIARY MEMORY BOARD AND EXPOSED TO THE UV LIGHT IN ACCORDANCE WITH THE MANUFACTURER'S INSTRUCTIONS. NOTE ALSO THAT EACH 2716 PROM CAN CONTAIN TWO INDEPENDENT TESTS WHICH WILL BOTH BE ERASED BY THE UV LIGHT.



PROM	1		2		3		4	
AUX. MEM. SELECT SWITCH POSITION	1	2	3	4	5	6	7	Not Used
PROGRAMMING ENABLE SWITCH POSITION	← 1 →		← 2 →		← 3 →		← 4 →	
2716 (2K UV PROM)	Test 1	Test 2	Test 3	Test 4	Test 5	Test 6	Test 7	Not Used
2758 (1K UV PROM)	Test 1		Test 2		Test 3		Test 4	

For example, to program test 4 when using 2716 PROMS, rotate the AUX. MEMORY SELECT switch to position 4 and activate programming enable switch no. 2. In order to program the 4th test when using 2758 PROMS, rotate the AUX. MEMORY SELECT switch to position 7 and activate programming enable switch no. 4.

Fig. 5.1.1.-4. AUX. MEMORY BOARD PROM programming details.

Step 38. B DATA CHANNEL SELF-TEST

The preceding self-test procedure for the A data channel will verify the proper operation of most of the analyzer functions and logic. In order to verify the remaining functions, an additional test using the B data channel should be made.

Turn power off and configure the analyzer as follows:

A channel probe - Insert into the A data channel connector. Set the TRUE/COMPLEMENT switch to TRUE and do not provide any input data to the A channel probe at this time. (Disconnect this probe from the SELF-TEST connector.)

B channel probe - Insert into B data channel input. Set the TRUE/COMPLEMENT switch to TRUE and using the self-test adaptor, connect the probe to the self-test port at the rear of the unit. MAKE SURE ALL LABELS ARE RIGHT-SIDE-UP.

Switch settings:

A CLOCK:	↓ (falling edge)
A QUALIFIERS:	Both X
B CLOCK:	↓ (falling edge)
B QUALIFIERS:	Both X
MEMORY SELECT:	Main
CLOCK/OFF/TRIG:	OFF

Step 39. POWER ON

Turn power on and note that the self-test software will configure the analyzer for OVERRIDE, the (A,B) triggering mode, and POS data collection. Note also that both A and B displays are blank. Press the TRIG key, activate the RESET switch, and set the A trigger word to XXXX (don't care). Press CTL and set the B trigger word to 0040. Then press CTL and SIG. Next rotate the DISPLAY TIME/HOLD control to HOLD and note that the ARM LED is on.

This is because the A clock is not connected and the B clock operates relative to the A clock.

Step 40. SIMULATING AN A DATA CHANNEL CLOCK

In order to trigger the analyzer, an input clock for the A data channel must be provided. This is accomplished by switching the A CLOCK SELECT switch (under the (A,B) LED) back and forth to simulate an incoming A CLOCK. Note that the ARM LED goes off indicating the analyzer has triggered. (If you can't get the analyzer to trigger, re-do Steps 38 and 39.)

Step 41. B DATA CHANNEL SELF-TEST SIGNATURE

Press CTL and place the analyzer in the SIG mode and compare the B self-test signature with the original A self-test signature at the front of the manual: they should be identical. (Ignore the current A signature since no meaningful data was collected.) Obtaining the correct self-test signature in this step verifies the B data channel trigger comparators, the clocking of the B data memory, and the operation of B data memory itself.

5.1.2 CHECK-OUT USING A SCOPE

The Model 532 will operate with most ordinary lab and field oscilloscopes with X(HOR), Y(VERT), and Z(BLANKING) inputs. If you're in doubt about your scope, check the required scope specifications in Section 2.0 or discuss them with the scope manufacturer or Paratronics, Inc. For example, some Philips scopes do not provide a blanking input (although they can be easily modified); and some older scopes require more than the 35V max blanking pulse provided by the Model 532 to fully blank the CRT. However, most TEK and HP scopes will give an excellent display. Fig. 5.1.2-1 shows the Model 532 with a typical lab scope.

Step 1. SCOPE CONNECTION

Connect the X(HOR), Y(VERT), and Z(BLANK) outputs of the Model 532 to the corresponding inputs on the scope. Set the scope's X and Y gain controls to approximately 0.5V/div.

Step 2. SETTING BLANKING POLARITY

Set the BLANK POLARITY SWITCH to the positive or negative sense in accordance with your scope's blanking requirements. (See Fig. 4.4-1 for the location of the BLANK POLARITY switches on the Model 532.)

> CAUTION
>
> BEFORE CONTINUING, BE CERTAIN THAT YOU DETERMINE WHAT THE BLANKING REQUIREMENTS OF YOUR SCOPE ACTUALLY ARE, OTHERWISE SERIOUS DAMAGE TO YOUR SCOPE'S BLANKING CIRCUITRY MAY RESULT. SEE SECTION 4.4 AND THE STEPS BELOW FOR ADDITIONAL INFORMATION.

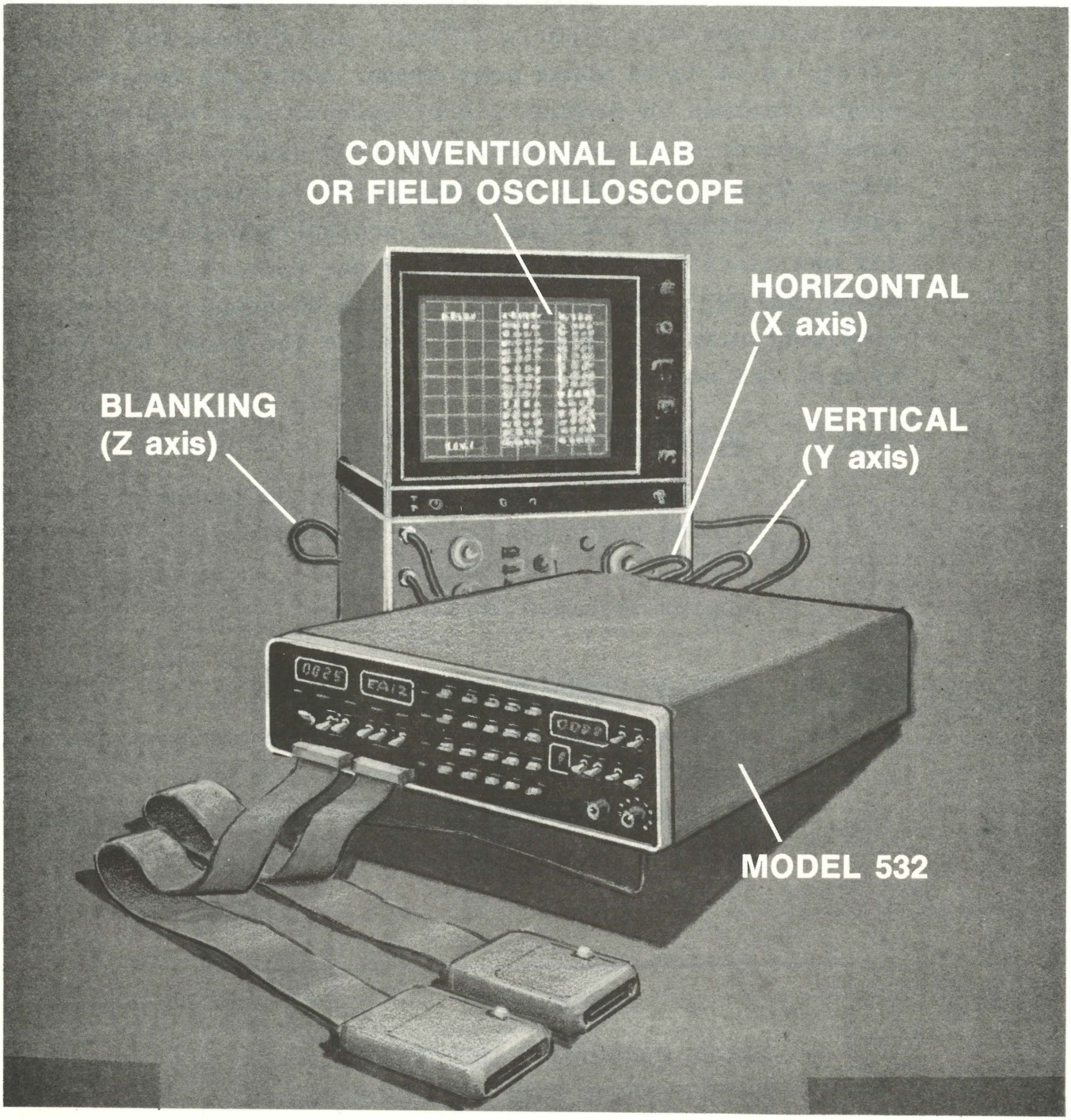


Fig. 5.1.2-1. The Model 532 with a typical scope.

Step 3. ADJUSTING BLANKING LEVEL TO MINIMUM

Rotate the BLANKING LEVEL ADJUSTMENT pot fully clockwise (CW) to the minimum output voltage position. (Fig. 4.4-1)

Step 4. INITIAL SET-UP AND TURN-ON

Perform Steps 1-9 in Section 5.1.1.

Step 5. XY DISPLAY ADJUSTMENTS

Use the scope's gain and positioning controls to get an image in the center of the CRT. If the ARM LED on the Model 532's front panel is illuminated, you will not get a display. If this is the case, review the procedure in Step 4 above. If the ARM LED still remains on, set both A and B trigger words to don't care (XXXX) and move the RESET/TRIG switch momentarily between the RESET and TRIG positions to force the Model 532 to display a truth table at random. Adjust the X and Y gain and positioning controls on the side of the Model 532 to fill the screen (Fig. 4.4.-1). (Note that additional adjustments of the scope's display controls may also be required.)

Step 6. BLANKING LEVEL ADJUSTMENT

Rotate the BLANKING LEVEL potentiometer counter-clockwise (CCW) until readable characters appear on the CRT.

CAUTION

TO REPEAT: DO NOT EXCEED THE MAXIMUM BLANKING VOLTAGE RECOMMENDED BY THE MANUFACTURER OF YOUR SCOPE.

Step 7. DISPLAY CLEAN-UP

Use the scope's focus, intensity, and astigmatism controls to obtain a bright, crisp, display. "Fine tune" the other controls discussed above, if necessary. See Figure 5.1.2-2.

> NOTE
>
> IF THE CHARACTERS ARE ROTATED OR TILTED, YOUR SCOPE HAS TOO MUCH PHASE SHIFT BETWEEN X AND Y: REFER TO THE SCOPE SPECIFICATION IN SECTION 2.0.

Step 8. SELF-TEST SIGNATURE VERIFICATION

If the signature-pair at the bottom of the CRT after initial power on corresponds with the values on the test tag and at the front of the manual, you may proceed; otherwise refer to Step 10 in Section 5.1.1.

Step 9. A TRIGGER WORD VERIFICATION

Perform Steps 11-15 in Section 5.1.1. Verify that the top 16-bit HEX word in the A section of the truth table matches the trigger word in the A display.

Step 10. CHANGING THE B TRIGGER WORD

Perform Steps 16 and 17 in Section 5.1.1.

Step 11. TESTING THE PARALLEL AND SEQUENTIAL TRIGGER MODES

Perform Steps 18-27. Note that a truth table display is present only when the ARM LED is off and that the delay value is displayed on the

CRT. (Fig. 5.1.2-2) Note also that for the POS (or post-trigger) examples used in these steps the first word in the data memory is always at the top of the truth table.

NOTE

TO AVOID CONFUSION, USE OF THE WORD MODE WHEN THE MODEL 532 IS CONNECTED TO A SCOPE IS NOT RECOMMENDED--USE THE PAGE FEATURE INSTEAD.

Step 12. USING THE PAGE CONTROL, POS MODE

INITIAL CONDITIONS: (A,B), TRIG, POS; A = 0040, B = FFFF, DLY = 0000, PAGE = 0

Rotate the DISPLAY TIME/HOLD control to the HOLD position. Increment the page number from 0 to 1 by momentarily pushing the PAGE UP/DN switch to the UP position. Note that the trigger locator at the upper left of the CRT changes from 0 to 16 and WORD 16 in the analyzer's data memory now appears at the top of the truth table, indicating that WORD 16 had occurred 16 clock pulses from the trigger. Next hold the PAGE UP/DN switch in the UP position to activate the page sweep mode. Note that any page from 0 to F (HEX) can be selected and that the memory "rolls over" to 0 after page F is displayed. Note also that page F contains only 10 words. (The remaining 6 words store the signature and front panel states for automatic operation.) Repeat the above procedure activating the DN position of the PAGE UP/DN switch. Then return to page 0.

Step 13. USING THE PAGE CONTROL WITH CLOCK DELAY, POS MODE

INITIAL CONDITIONS: (A,B), TRIG, POS; A = 0040, B = FFFF, DLY = 0000, PAGE = 0

Rotate the DISPLAY TIME/HOLD control counterclockwise so that the truth table flashes once or twice every second (about 10:00). (After each flash, a new data collection is performed; however, the data should be stable since the 8085 address is in a loop.) Increment the delay value to 0002. Next increment the page control to page 1. Note that the trigger locator at the top of the truth table has a value of +0018, indicating that the top word is 18 clock delays away from the trigger word. The algorithm used by the Model 532 for computing the trigger word locator in the POS mode is:

CLOCK DELAY VALUE + PAGE OFFSET = TRIGGER LOCATOR,

where the page locator depends on which page (0-F) is currently being examined.

PAGE	PAGE (POS MODE)
0	TRIG
1	+0016
2	+0032
3	+0048
4	+0064
5	+0080
6	+0096
7	+0112
8	+0126
9	+0144
A	+0160
B	+0176
C	+0192
D	+0208
E	+0224
F	+0240

The user is encouraged to experiment with different delay and page offset values to ensure a complete understanding of the operation of the Model 532 in the post-trigger mode.

Return to delay value 0000 and page 0.

Step 14. USING THE PAGE CONTROL WITH ZERO CLOCK DELAY, NEG MODE

INITIAL CONDITIONS: (A,B), TRIG, POS, A = 0040, B = FFFF, DLY = 0000, PAGE = 0

Press CTL followed by NEG to enter the pre-trigger collection mode. Decrement the PAGE UP/DN switch by one count for page F and note that the trigger word (0040,FFFF) is located at the bottom of the CRT (indicated by the label "TRIG.") In this case, this is the last word collected. Now increment the page to 0. The top word in the truncated truth table is the first word collected, or the 250th word prior to the trigger. (The -0240 locator value at the bottom of the truth table indicates that the associated word is occurring 240 clock pulses prior to the trigger.

NOTE

THE ABOVE TRUTH TABLE FORMAT FOR THE NEG MODE IS CONSISTENT WITH THAT USED FOR THE POS MODE: THE FIRST WORD COLLECTED IS ALWAYS AT THE TOP OF THE TRUTH TABLE IN PAGE 0, WHILE THE LAST WORD COLLECTED IS ALWAYS AT THE BOTTOM OF THE TRUTH TABLE IN PAGE F. IF THE USER REMEMBERS THIS CONVENTION, PARTICULARLY WHEN CLOCK DELAYS ARE USED DURING COLLECTION, INTERPRETATION OF THE DISPLAY WILL BE SIMPLER.

Step 15. USING THE PAGE CONTROL WITH NON-ZERO CLOCK DELAY, NEG MODE

INITIAL CONDITIONS: (A,B), TRIG, NEG, A = 0040, B = FFFF, DLY = 0000, PAGE = 0

Decrement the PAGE UP/DN switch by one count for page F. Again, note the trigger word (0040,FFFF) at the bottom of the page. Next, making sure that the CLOCK/OFF/TRIG switch is in the CLOCK position, increment the clock delay value to 0003. Note that the value (0042,FFFF) now appears at the bottom of the page along with the trigger locator value of +0003. Note also that the trigger word (0040,FFFF) has moved up the table by three places. This simple example indicates how the pre-trigger (NEG) mode can be used to view events before and after the trigger.

Now change the delay value to 0000 and the page to 0. Note the top three words in the truncated truth table. Again, increment the delay value to 0003 and observe how the words in the table again shift up three places. (The word which was previously fourth from the top is at the top.) Also note that the trigger locator at the bottom of the truth table changes to -0237 from -0240, indicating that the associated word is now occurring 237 clock pulses prior to the trigger.

Press CTL and set in a delay value of 0240 and observe that the trigger word now appears at the bottom of page 0. The following table shows how the trigger locator changes for various delay values:

CHANGE DELAY VALUE TO:	TRIGGER LOCATOR (Relative to page 0)	COMMENTS
0000	-0240	Trigger occurs 240 clock pulses later.
0239	-0001	Trigger occurs 1 clock pulse later.
0240	TRIG	Trigger occurs.
0241	+1	Trigger occurs 1 clock pulse earlier.
0249	+9	Trigger occurs 9 clock pulses earlier (top of truncated table).
9999	+9759	Trigger occurs 9759 clock pulses earlier.

The algorithm used by the Model 532 for computing the trigger word locator in the NEG mode is:

CLOCK DELAY VALUE - PAGE OFFSET = TRIGGER LOCATOR

where the PAGE OFFSET depends on which page (0-F) is currently being examined:

PAGE	PAGE OFFSET (NEG MODE)
0	-0240
1	-0224
2	-0208
3	-0192
4	-0176
5	-0160
6	-0144
7	-0126
8	-0112
9	-0096
A	-0080
B	-0064
C	-0048
D	-0032
E	-0016
F	TRIG

Step 16. TESTING THE TRIG DELAY

With the page set to 0 and the DELAY TIME/HOLD control in the HOLD position, set in a delay value of 0125 and change the CLOCK/OFF/TRIG switch to the TRIG position. For this set-up, the delay value refers to the number of times the trigger word must occur before the analyzer will trigger. Press RESET and note that the truth table disappears for approximately 4 seconds (125 counts). Then repeat this procedure in the positive mode by pressing CTL and POS. Finish this step with a delay value of 0000 and the CLOCK/OFF/TRIG switch in the CLOCK position.

Step 17. TESTING THE A CLOCK QUALIFIER

Rotate the DELAY TIME/HOLD control to approximately 10:00 and perform Step 34 in Section 5.1.1 (except do not enter the WORD mode--remain in the TRIG mode). Note that the resulting truth table contains only memory reference operations.

Step 18. TESTING THE A TRIG QUALIFIER

Perform Step 35 in Section 5.1.1, except do not enter the WORD mode. (Remain in the TRIG mode.) Note that because the analyzer is in the POS mode, the READ operation which enabled the triggering of the analyzer is at the top of the truth table.

Step 19. TESTING THE A BIN AND B BIN DISPLAY

Rotate the DISPLAY TIME/HOLD control to the HOLD position. Alternate the A BIN/HEX B switch between the HEX and A BIN position. Compare the A BIN machine language data with the hexadecimal equivlents of the A data channel. Repeat the above procedure with the B BIN machine language data and the hexadecimal equivalents of the B data channel.

MODEL 532 THEORY OF OPERATION

6.0 INTRODUCTION

The Model 532 is a sophisticated microprocessor-based, 32-channel logic state analyzer. Its versatile triggering capability and software control permit the instrument to be employed in a wide variety of applications. This section discusses the basic principles of operation only. No attempt is made to describe circuits in detail or the associated testing and troubleshooting procedures; these topics are covered along with schematic descriptions in the Model 532 Maintenance Manual.

6.1 GENERAL CONFIGURATION

Fig. 6.1-1 is a basic block diagram of the Model 532 showing how the key hardware and functional elements interface. Many of the subsystems--the X, Y display generator and the interface boards, for example--are separate hardware modules. Other parts of the system, such as those not required for custom applications, are integrated into the motherboard.

6.2 PROBES

The probes provide an electrical interface to the system-under-test. There are two types available for the Model 532: passive and active.

6.2.1 PASSIVE PROBES

The Model 50 (TTL threshold) and Model 51 (variable threshold) probes monitor the system-under-test and provide no stimulus or control functions (with the exception of the +5V and user-defined CNTRL output signals described in Sections 7.1.2 and 10.3). Generally, the probes provide buffering, noise rejection, and assure correct timing between clock, data, and qualifier signals. The circuitry of the Model 50 and Model 51 probes are powered through the flat ribbon interconnect cable. Both probes can be interfaced to the system-under-test using PC edge connectors, or through Model 52 probe terminator assemblies which incorporate color-coded flying leads with standard pin connectors at the ends. These connectors readily interface with wire-wrap pins, ball clips, or IC clips.

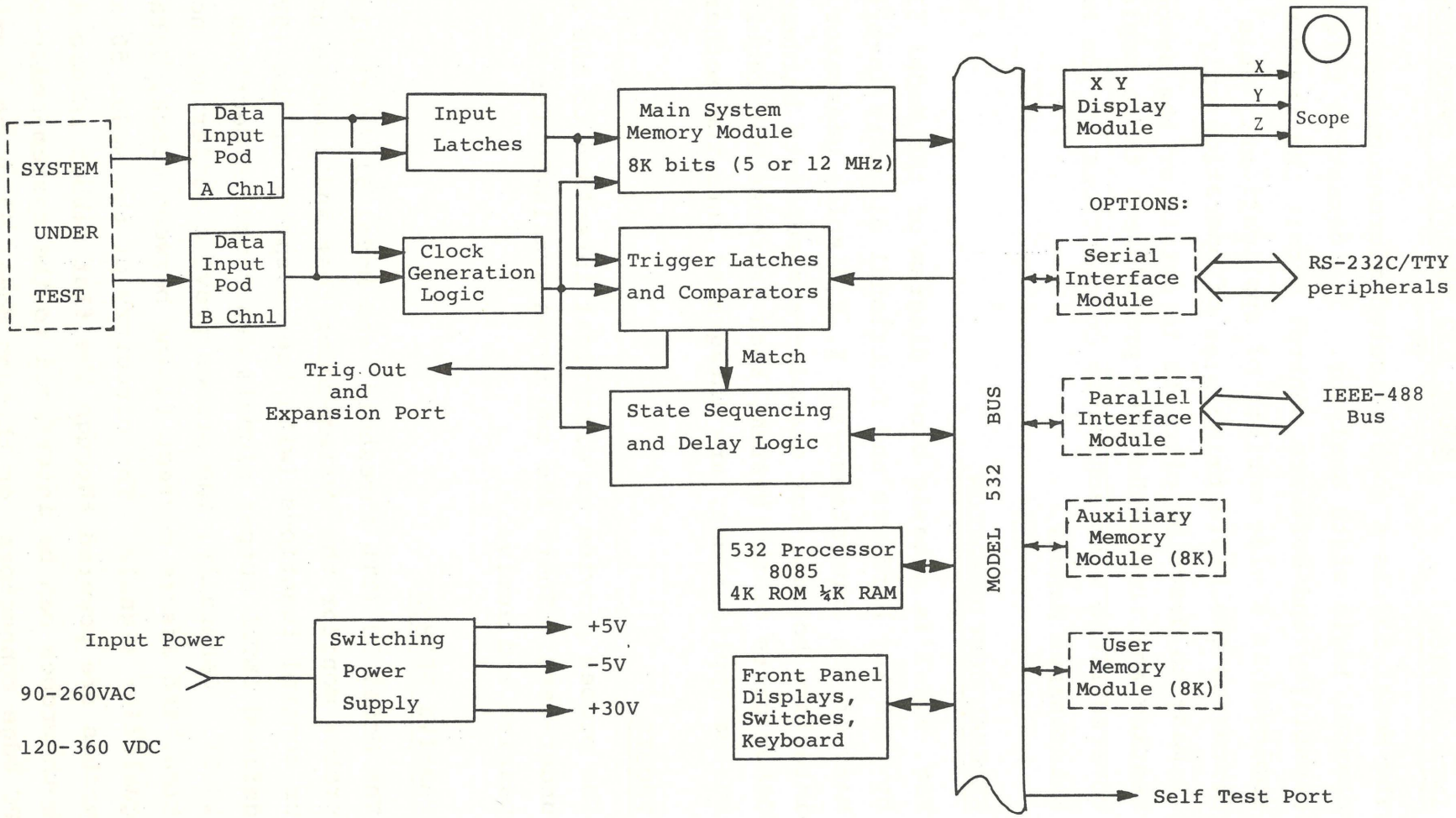


Fig. 6.1-1. Model 532 Logic State Analyzer Block Diagram.

6.2.2 ACTIVE PROBES

This probe type is dedicated to a specific microprocessor (e.g., 8080, 6800, etc.). It can provide active control as well as monitoring capability when plugged into the microprocessor socket of the system-under-test. (The microprocessor chip is then plugged into the dedicated probe itself.)

In this configuration, the dedicated probe provides buffering and data clock timing for standard logic analysis; it permits the Model 532 to perform READ and WRITE functions; it provides BREAKPOINT, RUN, and SINGLE-STEP control; and with the optional serial interface, it allows the user to examine the registers of the microprocessor-under-test. Additionally, a program in a portion of the User's Program Memory Board allows other development functions. (See Sections 11.0 and 6.15.)

6.3 INPUT LATCHES AND CLOCK GENERATION LOGIC

The input latches buffer data from the probes and condition it for storage into the main memory. The clock logic generates qualified write pulses for controlling the A and B sections of the main memory. These signals are also used to provide all internal clocking in the Model 532's state and sequencing logic.

6.4 MAIN MEMORY

The main memory performs all real-time data collecting. It is physically structured as 1K x 8 bits and is entirely contained on a Model 532 bus-compatible PC board. It interfaces with the input latches and is actually organized as two memories, each 16 bits wide and each 256 words deep. Thus, it is these two memories which record the data from the A and B data input channels, respectively. Note that MOS chips are used for the Model 532A (5 MHz) configuration and bipolar devices are used for the Model 532B (12 MHz) configuration.

6.5 TRIGGER LATCHES AND COMPARATORS

This circuitry compares data from the input latches with the contents of trigger latches which are loaded from the front panel via the Model 532 bus. When a match occurs, a signal is sent to the state sequencing and delay logic, described below. Note that triggering data consists of 3 separate open collector trigger signals which are brought out to the expansion port connector at the rear of the unit. This feature permits the "ganging" of two Model 532's for 64-bit triggering and analysis.

6.6 STATE SEQUENCING AND DELAY LOGIC

The state sequencing and delay logic processes the trigger signals and mode commands and directs operation of all analyzer subsystems. This logic is fully microprogrammed which provides the flexibility of altering the various Model 532 triggering modes for special applications.

6.7 MODEL 532 BUS

While not an actual subsystem itself, the Model 532 bus is the key interface to all major subsystems. It is a full computer bus which consists of 7 connectors located on the motherboard. All connector slots of the bus are electrically identical.

The Model 532 bus provides buffered TTL ADDRESS, DATA, STATUS, and INTERRUPT signals to all modules and subsystem interfaces. A description of all Model 532 bus signals is given in the Maintenance Manual.

6.8 FRONT PANEL

The Front Panel interfaces to the Model 532 bus so that the indicators, readouts, controls, and the keyboard are treated as I/O devices by the 8085 processor. This permits full flexibility in the adaptation of the indicators, readouts and controls for special, custom, operating modes. Two keys on the keyboard are available for user-defined functions.

6.9 MODEL 532 PROCESSOR

The Model 532 Processor consists of the 8085 CPU, 4K of ROM memory, 256 bytes of RAM memory, and associated buffering and interface logic. The processor directs all aspects of analyzer operation by performing the following tasks:

* Display generation and refresh
* Switch interpretation and debouncing
* LED display multiplexing
* Serial, and IEEE-488 interface control
* Trigger and mode control setup
* Analyzer state monitoring and control

6.10 XY DISPLAY BOARD

The XY display board also interfaces directly to the Model 532 bus. Under control of the processor, it positions characters on the CRT and "strokes" the beam to write each character. The display board also generates the necessary X (horizontal),Y (vertical),and Z (blanking) signals so character data can be presented on an ordinary oscilloscope.

6.11 POWER SUPPLY

The Model 532 power supply is an efficient, wide-range, switching supply. It can operate with input power from 90 to 260 volts AC or 120 to 350 volts DC. Size, weight and heat have been minimized in the design. The supply operates at 20 KHz and is fully shielded and EMI filtered. Normal output voltages consist of +5, -5 and +30 volts.

6.12 SERIAL INTERFACE (optional)

The Serial Interface Board (SIB) allows the Model 532 to communicate with standard RS-232C and TTY peripherals such as a teleprinter or keyboard/CRT. Remote operation can also be accomplished through the use of a modem to a remote terminal or computer. The baud rate is switch selectable from 50 to 9.6K baud. RS-232 or 20mA current loop full duplex interfaces can be accommodated. Detailed operation of the SIB is described in Appendix A.3.

6.13 IEEE-488 INTERFACE (optional)

The IEEE-488 interface board provides remote control and monitoring capabilities similar to the Serial Interface Board. It functions in both "talker" and "listener" capacities on the 8-bit parallel standard bus. Talker and listener addresses can be set into programming switches on the IEEE-488 interface board. The IEEE-488 interface is particularly useful for automating the Model 532 for production testing. Additional details are provided in Appendix A.4.

6.14 AUXILIARY MEMORY (optional)

Using 1K bytes of RAM and 7K bytes of PROM (out of 8K bytes on the board), the Auxiliary Memory permits 8 independent data collections to be stored (via the Model 532 bus) for later comparison with the main memory. The board also contains the required PROM programming circuitry for 2716-type UV PROMS. Under the direction of keyboard commands, a software routine allows the saving of a full 32 x 250 data collection as well as the associated signatures and the front panel states used in the original data collection. Upon recall of the contents of the auxiliary memory, the front panel states are duplicated and the operation of the Model 532 is now automatic. After new data are collected, the signatures and the 32 x 250 data words in the main memory are compared with the previous collection in the auxiliary memory and any differences are flashed on the CRT. Note that the HOLD $\neq$ trigger mode automatically halts a data collection if the main and auxiliary memories disagree. This mode is extremely useful for locating intermittent faults.

Additional auxiliary memory software checks to see if the selected UV PROM is blank before permitting the programming operation. Furthermore, PROGRAMMING VOLTAGE ENABLE switches on the board itself serve as an extra precaution in the field where a UV light source for erasing erroneously programmed PROMS may not be readily available.

6.15 USER MEMORY (optional)

The User's Memory Board is virtually identical to the Auxiliary Memory Board in terms of its RAM and UV PROM capacity. The main difference is that it occupies a different address space on the Model 532 bus. It's purpose is to provide the user with a means of incorporating special functions into the Model 532. By writing appropriate 8085 code, the user can:

* Define a custom function for each of the two spare keys on the keyboard.

* Redefine any other front panel switches and keys.

* Design special display formats.

* Incorporate custom automatic functions.

When used with the dedicated probe, a special section of the User's Memory Board is preprogrammed at the factory to provide enhanced special microprocessor development functions such as:

* Microprocessor internal register trace and display.

* Disassembly of collected data.

7.0 CONNECTION TO THE SYSTEM-UNDER-TEST

The Model 532 can be interfaced in a variety of ways --which way the user chooses depends on his particular application and the mechanical configuration of the system-under-test.

> **CAUTION**
>
> WHEN INTERFACING TO THE SYSTEM-UNDER-TEST, ALWAYS CONNECT THE GROUND LEAD OF THE PROBE FIRST TO INSURE THAT BOTH CHASSIS' SHARE A COMMON GROUND POTENTIAL. THIS MINIMIZES THE CHANCE FOR DAMAGE DUE TO STATIC, FLOATING GROUNDS, OR AC COUPLING OF THE INPUT SIGNALS. ALSO, THE GROUND LINE SHOULD ALWAYS BE REMOVED LAST.

7.1 MECHANICALLY INTERFACING THE MODEL 50 AND 51 PASSIVE PROBES

Both the fixed TTL threshold Model 50 and the variable threshold Model 51 probes interface to the system-under-test using a Model 52-series probe terminator for existing systems, or to a PC board edge connector (or maintenance port) incorporated into newer systems specifically to support troubleshooting with a logic analyzer. (See Fig. 7.1-1.)

7.1.1 THE MODEL 52 PROBE TERMINATOR

The Model 52 probe terminator is plugged into the Model 50 or Model 51 probe when it is desirable to take advantage of the full interconnection capability offered by the flying leads. Each terminator has 20 color-coded leads providing the following functions: data inputs (16); trigger and clock qualifiers (2); clock (1), and ground (1). Each lead has a wire color plus a tip color for positive identification. Fig. 7.1.1-1 is a reproduction of the color-code definitions provided on the Model 52 probe terminator label.

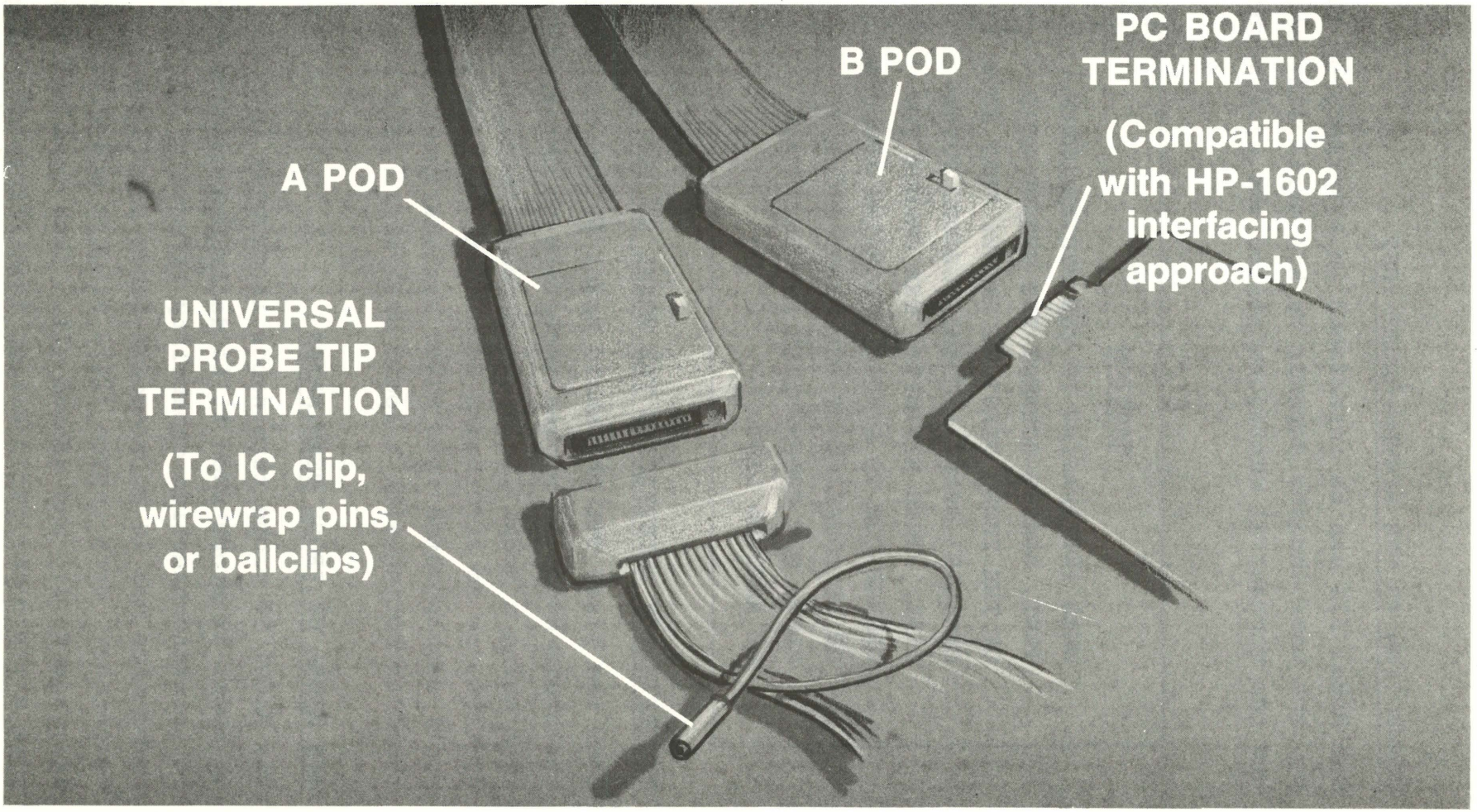


Fig. 7.1-1. Model 532 probes and interfacing techniques. Note that other probe tips are available.

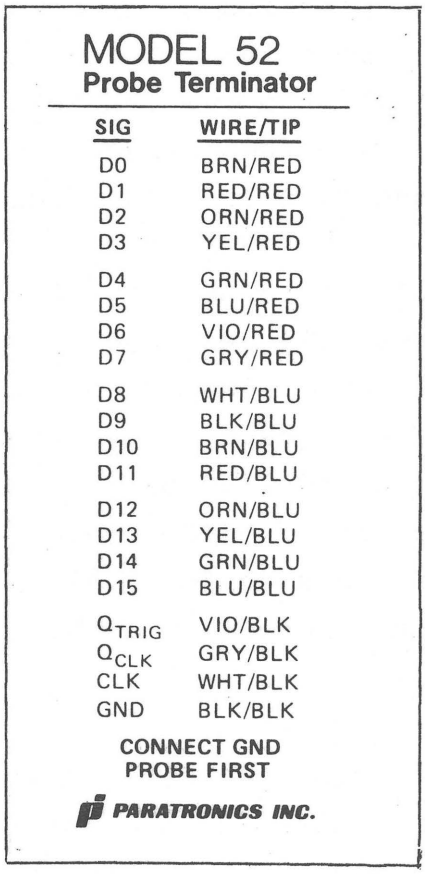


Fig. 7.1.1-1. The Model 52 Color Code.

The Model 52-1 probe terminator is shown in Fig. 7.1.1.-2. Note that each flying lead is terminated in a gold-plated Berg pin which readily mates with wirewrap pins, IC clips and ball clips. (The Model 52-2 is terminated in miniature ball clips; and the Model 52-3 is unterminated.)

7.1.2 DIRECT INTERFACING WITH A MAINTENANCE PORT

In order to simplify system test, there is a growing trend towards incorporating "maintenance ports" into new product designs. These ports bring out critical monitoring signals and allow analysis equipment, such as the Model 532, easy access to system operation by directly plugging a Model 50 or 51 data input probe into compatible PC board edge fingers. Fig. 7.1.2-1 illustrates the concept and mechanical requirements associated with the maintenance port. Note the offset arrangement of the PC board edge fingers which prevent the Model 50 or 51 probes from being inserted backwards. Also note that the Model 50 or 51 probes are compatible with maintenance ports presently designed for use with the HP-1602A Logic State Analyzer. However, due to the fact that the Model 532 offers more capability, a maintenance port designed to accommodate the Model 50 or 51 probes may not be useable with the HP-1602 probe. (The primary difference between the two configurations is that the Model 532 offers a trigger qualifying signal and a CNTRL signal not available on the HP-1602A.)

The Model 50 and 51 probes also offer a +5V output which can drive external circuit loads up to 200mA. Use of the +5V and/or the CNTRL signal allow special automatic control and sense functions to be implemented when the probe is connected to the maintenance port. Note that these active signals are not brought out on the probe terminator's flying leads in order to avoid the accidental connection to sensitive circuitry in the system-under-test.

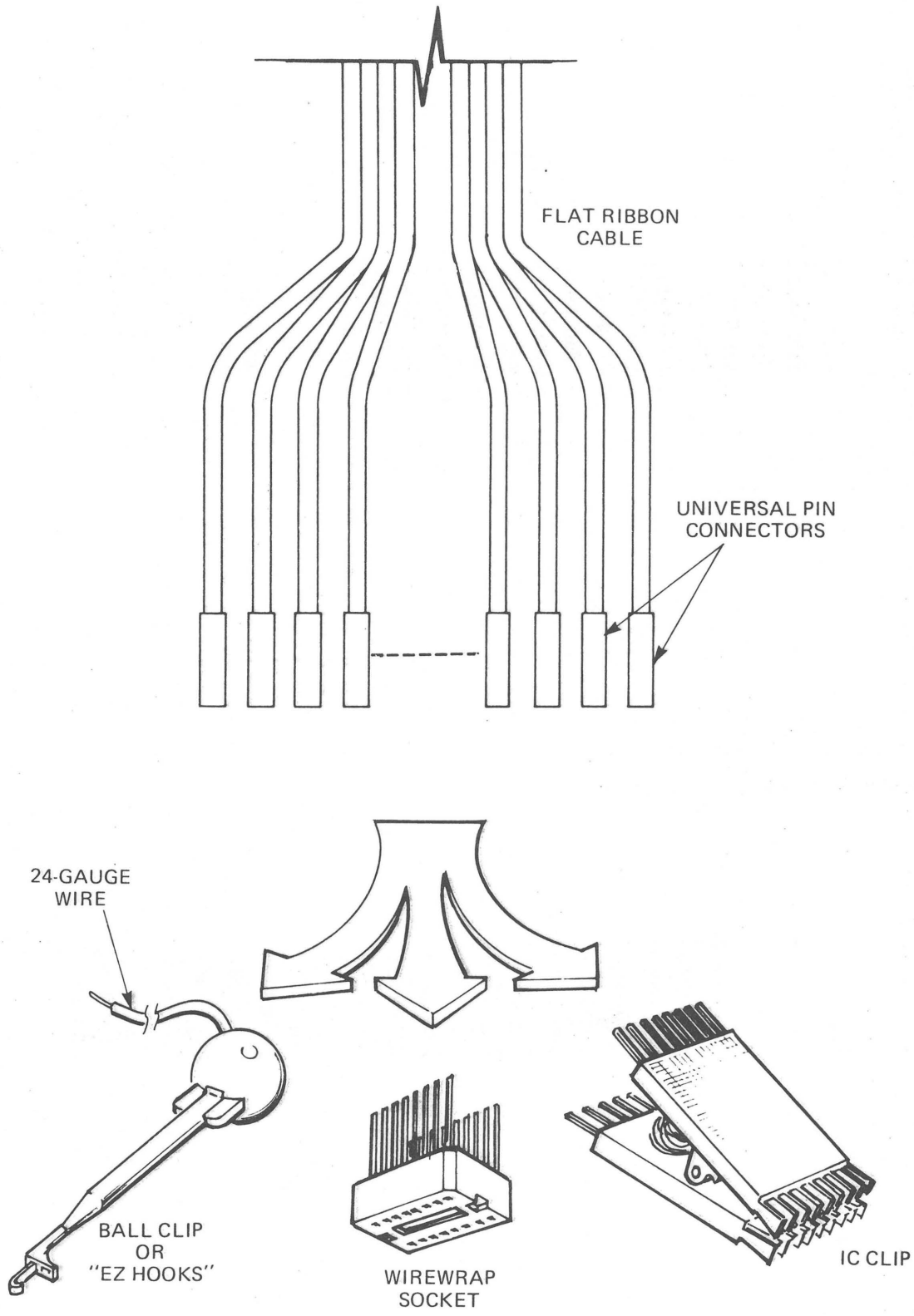
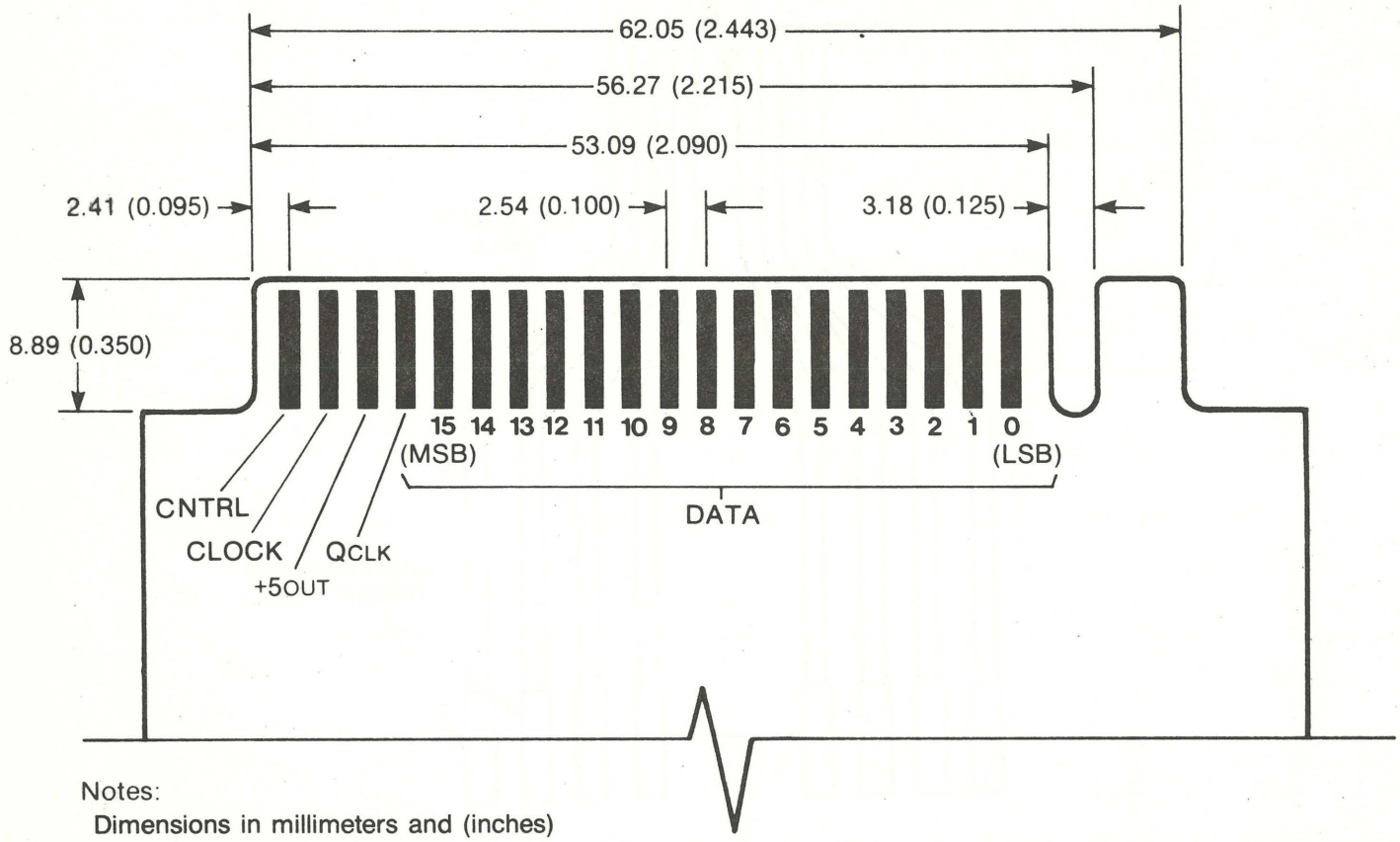


Fig. 7.1.1-2. Use of "Universal Pin Connectors" (Berg pins) for system interconnection.



Notes:
Dimensions in millimeters and (inches)
1.57 (0.062) thick PC Board
Dimension Tolerance = 0.13 (0.005)

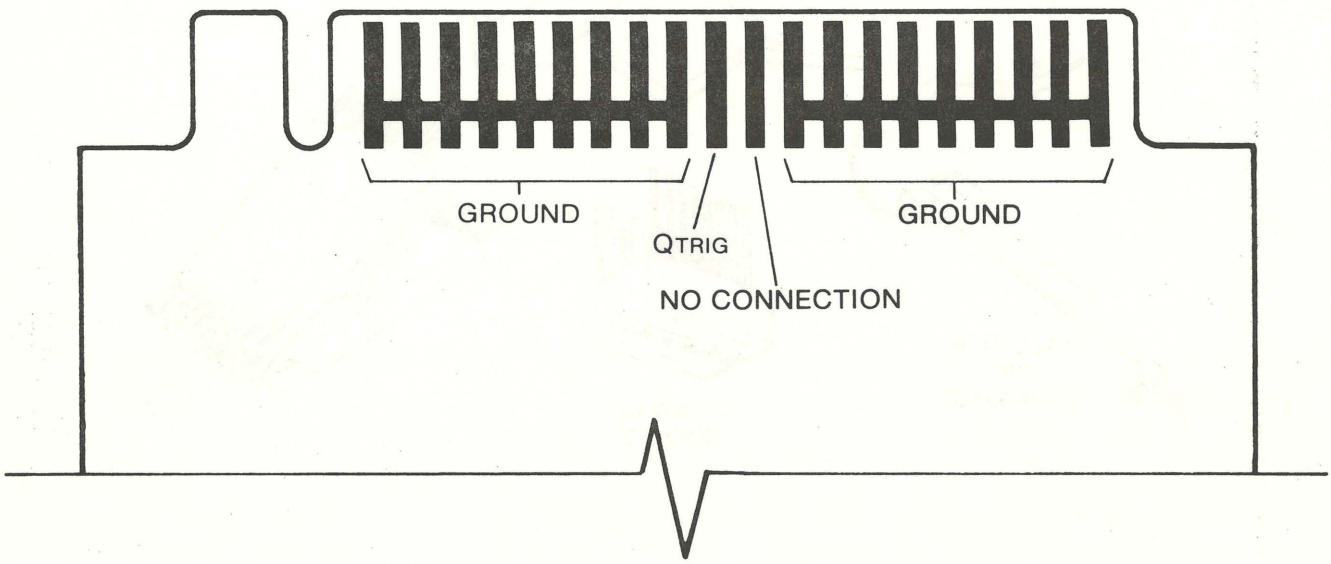


Fig. 7.1.2-1. Electrical and mechanical definitions of the Model 532 Maintenance Port.

7.1.2.1 MAINTENANCE PORT DESIGN GUIDELINES

The maintenance port should be defined so that the most important test signals are available for monitoring. Of course, even through as many as 32 signals can be monitored by the Model 532, the designer should consider implementing additional test ports and moving the Model 532's probes around for monitoring the highest number of test signals possible. Typical signals which sould be considered for bringing out on the maintenance port include:

* Computer or microprocessor address bus
* Memory and I/O data busses
* Status and control signals
* Output from system sensors
* Inputs to system activators
* Key points in a combinatorial logic network
* Control memory address bus (microprogrammed machines)
* Microcontrol word (microprogrammed machines)

Consideration should also be given to the use of clock and trigger qualifier signals. These signals can be used to provide additional control of analyzer sampling and triggering. Since all qualifier inputs can be switched to don't care (X) from the Model 532 front panel, the use of these signals in no way restricts the triggering of the Model 532.

7.2 ELECTRICALLY INTERFACING THE MODEL 50 AND MODEL 51 PROBES

CAUTION

IT IS IMPORTANT TO OBSERVE THE FOLLOWING MAXIMUM INPUT VOLTAGE RANGES TO AVOID DAMAGE TO THE PROBES:
MODEL 50 (FIXED THRESHOLD): -0.5V to +15V
MODEL 51 (VARIABLE THRESHOLD): ±25V
ALSO, ALWAYS CONNECT THE BLACK GROUND PROBE WIRE FIRST AND REMOVE IT LAST.

Note: If a probe is inadvertently damaged, it can be easily repaired by dismantling the plastic covers and replacing the damaged IC's. (All IC's are in sockets.) Refer to the Maintenance Manual for additional trouble-shooting and repair information.

7.2.1 INPUT SIGNAL AND LOADING CHARACTERISTICS

In order to ensure reliable logic state analysis, the user should be familar with the input loading and threshold characteristics of the various probe types.

7.2.1.1 SIGNAL LEVELS FOR THE MODEL 50 PROBE

Although the Model 50 input circuits have a fixed threshold input optimized for TTL logic, the probe can also be used for logic families, such as CMOS, which switch between 0 and up to +15.0V. Each probe input represents one low-power Schottky load as follows:

INPUT VOLTAGE	CURRENT
-.5V to +.8V	400 µa max. sourced from the probe.
+2.0V to +15V	100 µa max. sourced from the circuit-under-test.

Note that the associated equivalent shunt capacitance is $\leq$ 15pF on all inputs.

Note also that all data and qualifier inputs incorporate 400 mV (min.) of hysteresis for noise rejection and the threshold is fixed at approximately 1.6V.

NOTE

THE INPUT CLOCK CIRCUITRY DOES NOT INCORPORATE HYSTERESIS DUE TO TIMING CONSTRAINTS; THEREFORE, THE SYSTEM CLOCK USED SHOULD BE RELATIVELY "CLEAN" AS IT CROSSES THE THRESHOLD REGION OF 1.6V.

With the TRUE/COMPLEMENT switch in the TRUE position, input voltages associated with data and qualifier inputs of +2.0V to +15.0V are considered by the Model 532 as logic ONE's; and voltages between -0.5V and +0.8V are logic ZERO's. With the switch in the COMPLEMENT position, the logic senses are reversed. Note that the clock input is not affected by the TRUE/COMPLEMENT switch, but only by the CLOCK EDGE SELECT (⌐ or ¬) switch.

7.2.1.2 SIGNAL LEVELS FOR THE MODEL 51 PROBE

Whereas the threshold is fixed for the Model 50 probe, the Model 51 features a continuing variable threshold between ±15V. The threshold value is set using a potentiometer with a slotted shaft accessible through a hole in the probe case. A voltage monitoring point (with respect to ground) is also provided so that accurate threshold values can be established.

NOTE

THE VOLTAGE AT THE MODEL 51'S MONITORING POINT IS 20% OF THE ACTUAL THRESHOLD VALUE. THUS, A MONITORING POINT VOLTAGE OF +1.0 VOLTS WILL YIELD AN ACTUAL THRESHOLD VALUE OF +5.0V. THE THRESHOLD VALUE IS ADJUSTABLE BETWEEN ±15.0V.

The following table provides additional information about the input characteristics of the Model 51.

CHARACTERISTIC	VALUE
MINIMUM SIGNAL SWING	0.6V
THRESHOLD ACCURACY	±200mV
INPUT RESISTANCE	50Kohms
INPUT CAPACITANCE	15pF

The Model 51 probe incorporates a resistance divider in front of the input sense amps so that resistor ratios can be tailored to accommodate different logic swings such as those associated with low-level logic or even 24V and 48V logic circuits. (Consult the factory about special threshold versions of the Model 51.)

The Model 51 features a fixed threshold TTL switch which permits the user to set the probe to a threshold value of +1.6V ± 200 mv without disturbing the variable setting.

The Model 51 also features a TRUE/COMPLIMENT switch. With the TRUE position selected, all input data and qualifier signals at least 300mV above the threshold will be considered logic ONE's; and all signals a least 300mV below the threshold will be logic ZERO's. In the COMPLIMENT position, the logic senses are reversed. Note that the input clock is not affected by this switch.

The Model 532 can accept two data input probes for 32-channel operation. Since the instrument is functionally split into two 16-channel A and B data input groups, any mix of threshold settings and logic senses can be used to accomodate a variety of system requirements.

NOTE

DUE TO TIMING CONSTRAINTS, THE MIXING OF A MODEL 50 PROBE AND A MODEL 51 PROBE IS NOT RECOMMENDED. IF A PROBE MIX MUST BE USED, THE MODEL 50 MUST BE PLUGGED INTO THE A DATA CHANNEL AND THE MODEL 51 INTO THE B DATA CHANNEL.

7.3 INPUT SIGNAL TIMING

Fig. 7.3.-1 illustrates the input signal timing requirements for both the Model 50 and Model 51 probes. If the user is sure that the system-under-test meets or exceeds the minimum values specified, the Model 532 will reliably collect data; otherwise data collection errors may occur.

7.4 RESET SYNCHRONIZATION

After a manual or automatic reset (see Section 10.6), one clock pulse is required from the system-under-test to remove the reset condition. This is necessary to ensure proper reset synchronization and eliminate the possibility of false triggering. If it is essential to collect data on the first clock cycle of the system-under-test (as is necessary when monitoring a power-up sequence, for example), a single clock which removes the reset condition can be simulated by toggling the A CLOCK SELECT switch one time.

7.5 MANUAL TRIGGER

The manual trigger on the 532 is used to force a trigger condition when fewer than the normal 250 words have been collected. As described in Section 7.4, a single clock pulse which synchronizes the reset must be received before the manual trigger can be activated.

After a manual trigger, the display data is interpreted as follows:

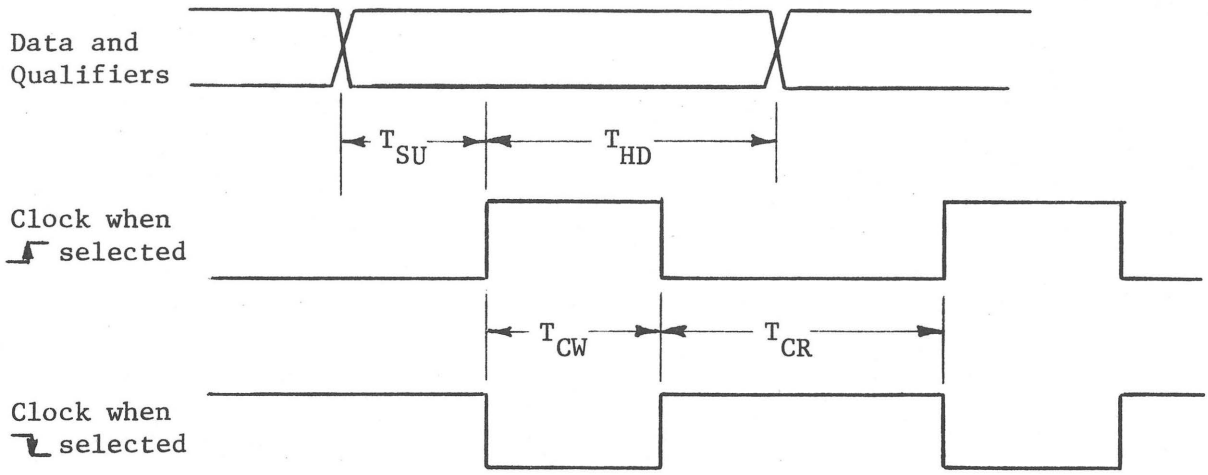
Positive Time (post-trigger) Modes:

Condition 1. The trigger word and two or more words are collected. All valid words collected will be displayed. Any invalid word in the memory will be blanked.

Condition 2. The trigger word has not occurred, or fewer than two words have been collected after the trigger word. In this case, three words will be displayed where the words preceding the trigger word are invalid.

Negative Time (pre-trigger) Modes:

By definition, the triggering conditions have not been met if manual trigger is required in negative mode. Thus, the display contains all valid words. Invalid words are blanked.



SYMBOL	DESCRIPTION	VALUE
T_{SU}	Data and Qualifiers Setup	30ns
T_{HD}	Data and Qualifier Hold	0ns
T_{CW}	Active Clock Pulse Width	20ns (min)
T_{CR}	Clock Recovery Pulse Width	30ns (min)
	(All times referred to threshold crossing)	

MAXIMUM CLOCK FREQUENCY: 532A -- 5 MHz
532B -- 12 MHz

Fig. 7.3-1. Models 50 and 51 probe timing requirements.

8.0 TRIGGERING MODES

In this section, a complete description of each of the Model 532's 21 triggering modes is provided. These descriptions include typical uses, display interpretation information, and TRIG output pulse timing information in the format described below.

8.1 TRIGGER DESCRIPTION

Each triggering mode is described in a format which identifies the relationship between A, B and the associated delay. Note that the Model 532 has two main types of triggering modes:

1. Parallel Modes - A and B are concatenated to specify a 32-bit trigger word.
2. Sequential Modes - A refers to an event which occurs in the A data channel, while B refers to a later event which also occurs in the A data channel. (This mode is often used to monitor address execution sequences.)

8.2 TYPICAL USES

For each triggering mode, a typical use is suggested. However, as more familiarity with the Model 532 is gained, additional applications will become evident.

8.3 DISPLAY INTERPRETATION

This is a paragraph which describes the display after triggering. For the POS (post-trigger) mode, the data and the associated delay from the trigger for the first word collected are described. For the NEG (pre-trigger) mode, this description is for the last word collected. Note that these descriptions apply for both stand-alone and CRT display presentations. For stand-alone display, the word locator (delay value) in the WORD mode is assumed to be 0000. For use with a CRT display, the first word collected is

always at the top of page 0 and the last word collected is always at the bottom of page F.

8.4 STATE DIAGRAM

The Model 532 contains a microprogrammed state sequencer which directs the analyzer through the various states required to accomplish correct triggering. For each triggering mode, a simplified state diagram representing sequencer activity is provided to help the user understand the mode. There are four states involved:

1. RESET: This state is entered when a software reset occurs as a result of a display timeout in the repetitive display mode, or upon user activation of the RESET switch on the front panel.
2. CONTINUE: This is a multi-function state which is entered while the analyzer is waiting for the data memory fo fill up.
3. DELAY: This state is entered while the analyzer is waiting for the delay values to count down.
4. DISPLAY: This state is entered when data collection is complete and the analyzer is displaying data and is indicated by the ARM LED being off. Note that user activation of the TRIG position of the RESET/TRIG switch will always force the analyzer into the DISPLAY state.

There are several state transitions (Fig. 8.4-1) which are common to all modes. For simplicity, these transitions are not shown on the individual triggering mode state diagrams.

8.5 TRIGGER OUTPUT

Each triggering mode description includes a basic timing diagram to aid in interpreting the TRIG output pulse. This pulse is a low-going TTL level (20 mA sink) available at a rear panel BNC connector. The level is low whenever the

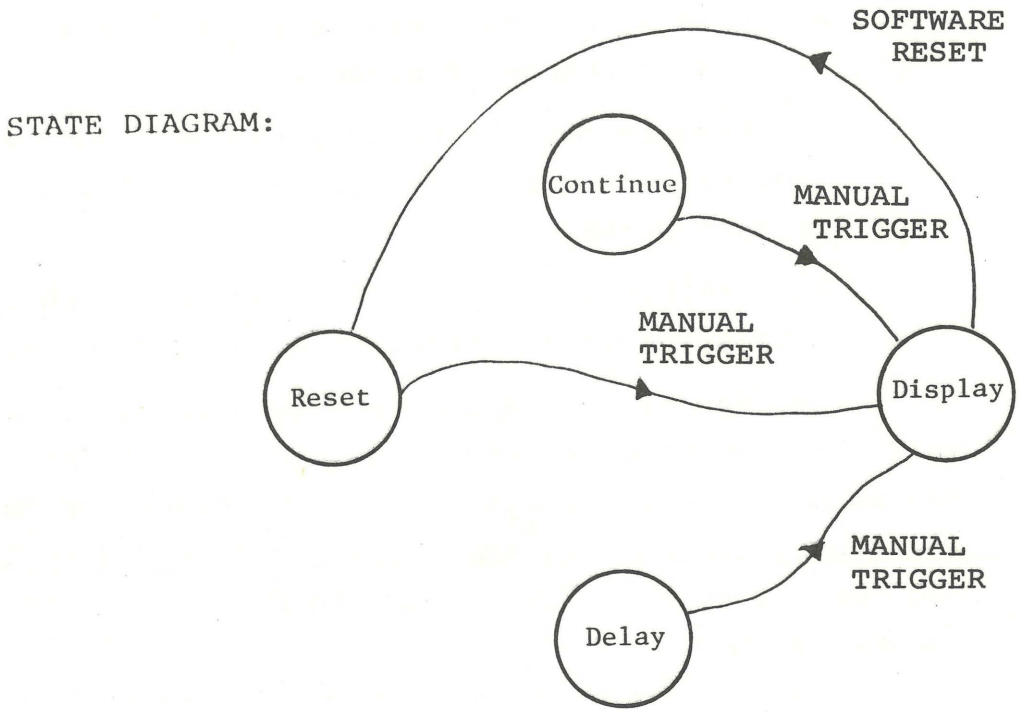


Fig. 8.4-1. State transitions common to all triggering modes.

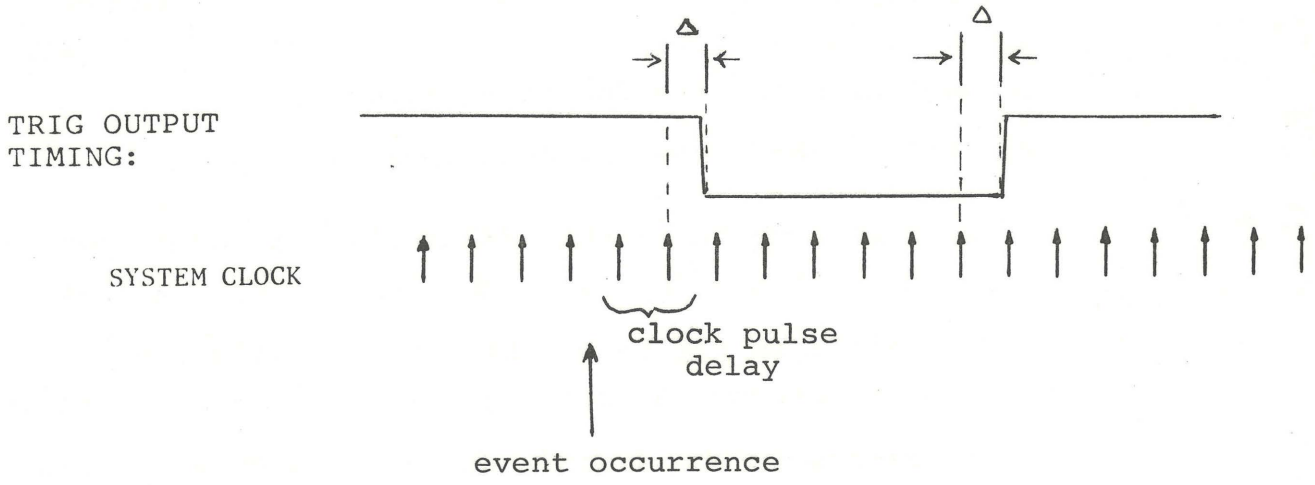


Fig. 8.5-1. Internal delays associated with the TRIG output.

analyzer is in the DELAY state. Typical uses for the TRIG output are:

1. Waveform or timing analysis related to a digital state or sequence of events.
2. Performance monitoring of parameters such as the frequency of occurrence of a particular instruction or subroutine.
3. Performance monitoring of parameters such as the time spent in a particular code block or subroutine.

The transition of the TRIG output is delayed from the initiating event by clock pulses plus an internal delay. The number of clock pulse delays are evident on the individual timing diagrams. This internal delay is fixed and identified by a "Δ" symbol in Fig. 8.5-1 and has these nominal values:

MODEL	MAX FREQ	NOMINAL
532 A	5 MHz	200 ns
532 B	12 MHz	100 ns

8.6 DEFINITIONS OF A, B, AND n

The following pages describe each of the 21 triggering modes: parallel triggering modes are described first; sequential modes are described second.

For all of the following descriptions:

A refers to the 16-bit HEX trigger value in the A data window "ANDed" with the A trigger qualifier.

B refers to the 16-bit HEX trigger value in the B data window "ANDed" with the B trigger qualifier.

n refers to the 4-digit decimal value in the DELAY COUNT readout.

MODE 1

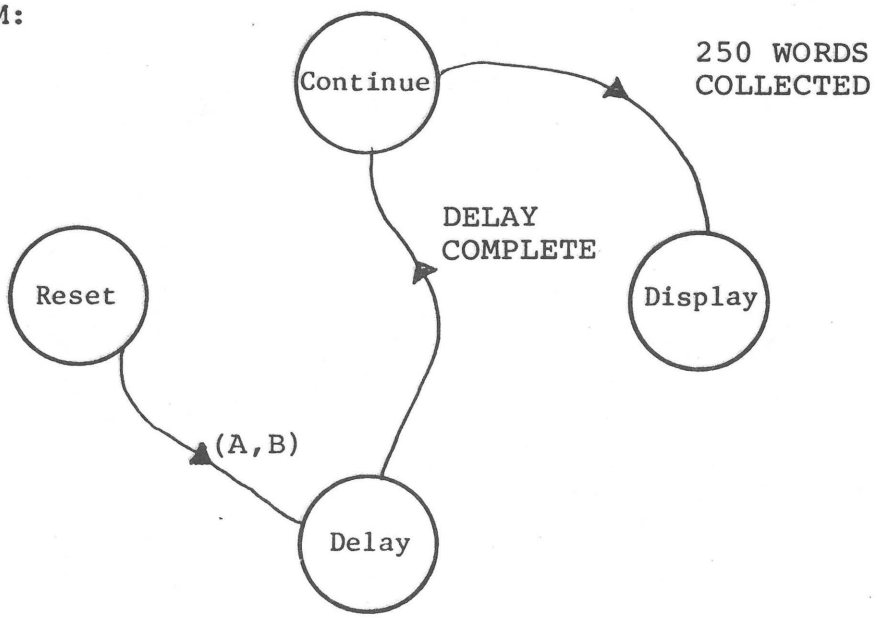
PARALLEL TRIGGER MODE: (A,B), POS, N CLOCK DELAYS

DESCRIPTION: INITIATE A 250-WORD DATA COLLECTION n CLOCK CYCLES AFTER THE OCCURRENCE OF A 32-BIT TRIGGER WORD CONSISTING OF A CONCATENATED WITH B.

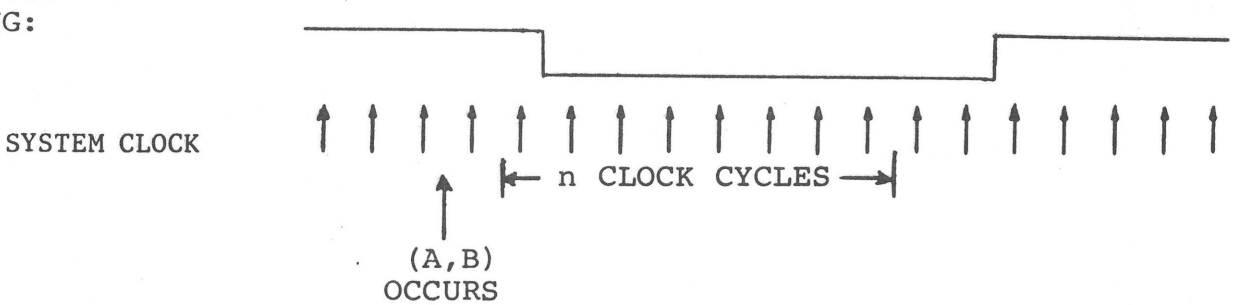
TYPICAL USE: TRIGGERING ON A 32-BIT (OR SHORTER) DATA WORD OR AN ADDRESS/DATA COMBINATION.

DISPLAY: THE FIRST WORD COLLECTED WILL OCCUR n CLOCK CYCLES FROM THE TRIGGER (A,B), AS INDICATED BY THE TRIGGER LOCATOR AT THE TOP OF PAGE 0.

STATE DIAGRAM:



TRIG OUTPUT TIMING:



MODE 2

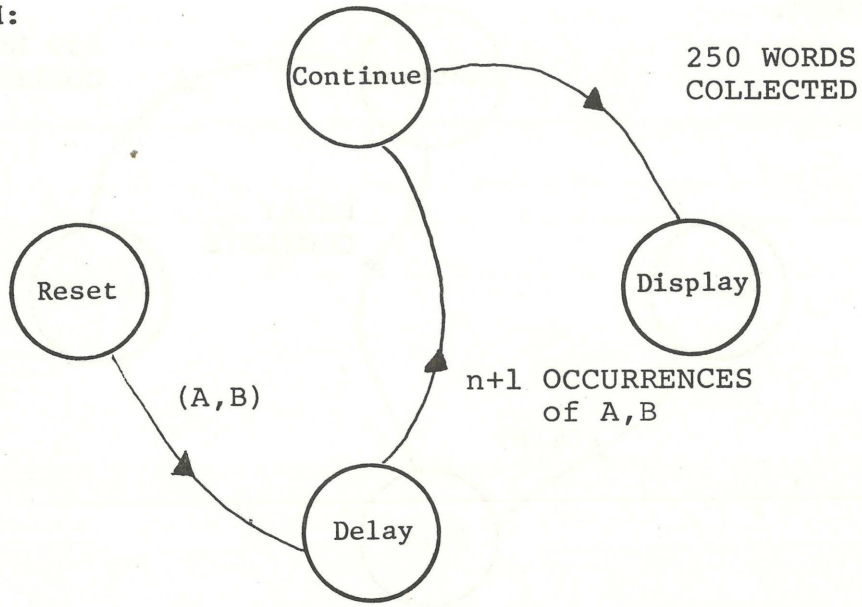
PARALLEL TRIGGER MODE: (A,B), POS, N TRIG DELAYS

DESCRIPTION: INITIATE A 250-WORD DATA COLLECTION AFTER DELAYING n OCCURRENCE OF THE 32-BIT TRIGGER WORD CONSISTING OF A CONCATENATED WITH B.

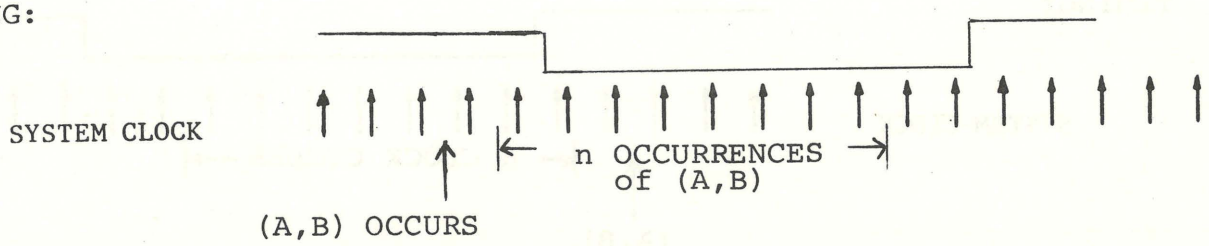
TYPICAL USE: FOR TRIGGERING AND COLLECTING DATA AFTER n PASSES THROUGH AN ADDRESS/DATA PAIR. USEFUL FOR COMPUTER PROGRAM LOOP ANALYSIS.

DISPLAY: THE FIRST WORD WILL BE COLLECTED AT THE (n+1) OCCURRENCES OF (A,B). THE CLOCK DELAY OFFSET WILL BE 0 AS IDENTIFIED BY THE "TRIG" LABEL ON THE FIRST LINE OF PAGE 0.

STATE DIAGRAM:



TRIG OUTPUT TIMING:



MODE 3

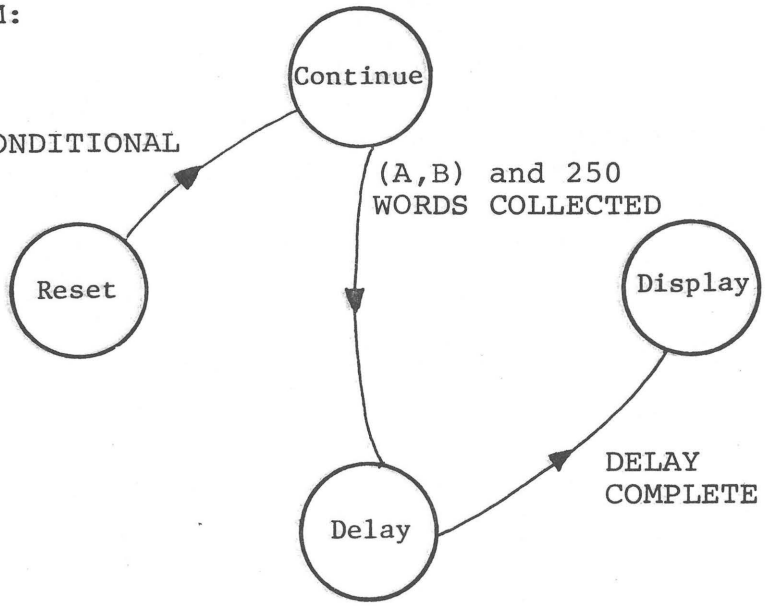
PARALLEL TRIGGER MODE: (A,B), NEG, N CLOCK DELAYS

DESCRIPTION: HALT DATA COLLECTION n CLOCK CYCLES AFTER THE 32-BIT TRIGGER WORD CONSISTING OF A CONCATENATED WITH B OCCURS.

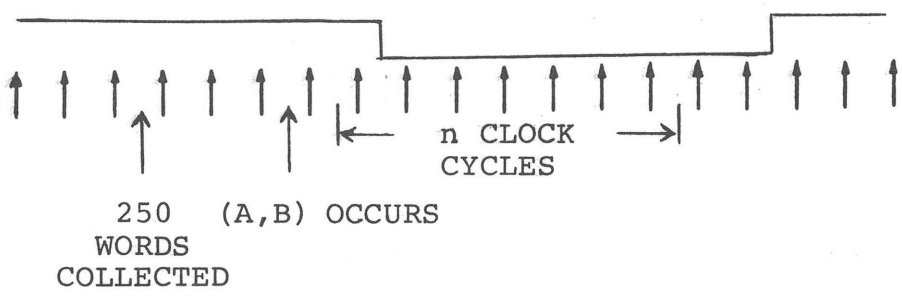
TYPICAL USE: FOR TRIGGERING ON A 32-BIT (OR SHORTER) DATA WORD OR AN ADDRESS/DATA COMBINATION AND VIEWING DATA OCCURRING BEFORE THE TRIGGER WORD. WHEN A DELAY OF LESS THAN 249 IS USED, DATA PRECEDING AND FOLLOWING THE TRIGGER WORD ARE COLLECTED.

DISPLAY: THE LAST WORD COLLECTED WILL BE THE WORD WHICH OCCURRED n CLOCK CYCLES AFTER THE TRIGGER WORD (A,B). THE CLOCK DELAY OFFSET WILL BE +n AS INDICATED BY THE TRIGGER LOCATOR AT THE BOTTOM OF PAGE F.

STATE DIAGRAM:



TRIG OUTPUT
TIMING:



MODE 4

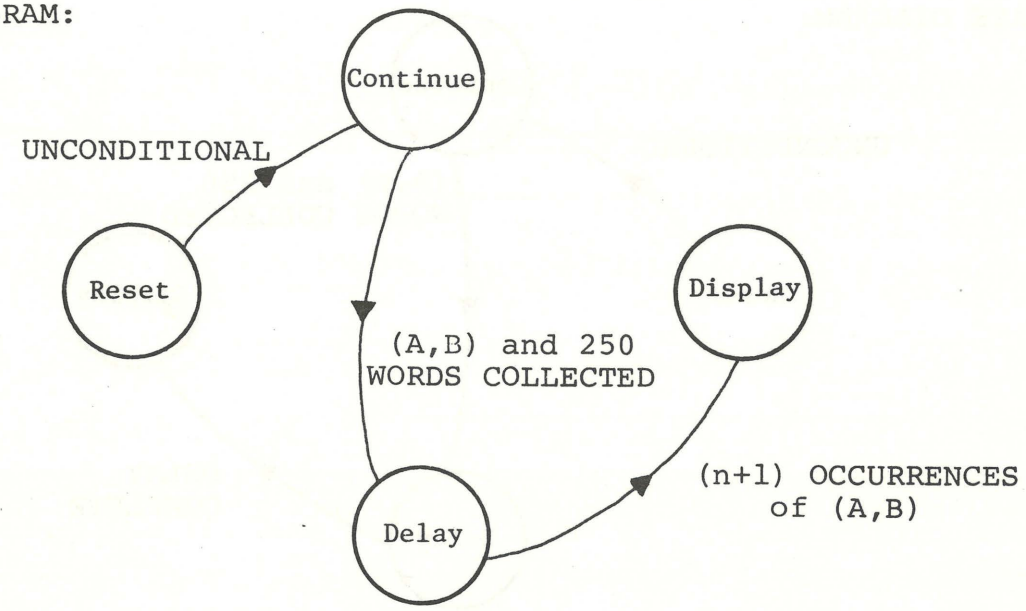
PARALLEL TRIGGER MODE: (A,B), NEG, N TRIG DELAYS

DESCRIPTION: HALT DATA COLLECTION AFTER DELAYING n OCCURRENCES OF THE 32-BIT TRIGGER WORD CONSISTING OF A CONCATENATED WITH B.

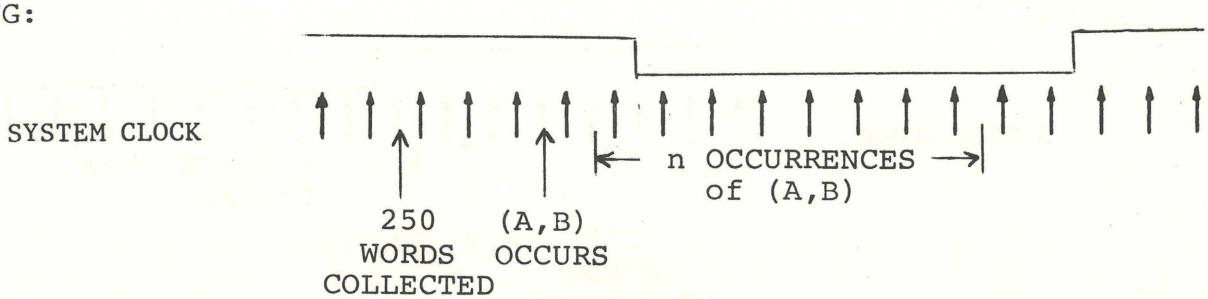
TYPICAL USE: FOR VIEWING ADDRESS AND DATA TRANSACTIONS OCCURRING IMMEDIATELY BEFORE A SPECIFIC PROGRAM LOOP.

DISPLAY: THE LAST WORD IS COLLECTED AT THE $(n+1)^{st}$ OCCURRENCE OF THE TRIGGER WORD (A,B). THE DELAY OFFSET IS 0 AS IDENTIFIED BY "TRIG" AT THE LAST WORD OF PAGE F.

STATE DIAGRAM:



TRIG OUTPUT TIMING:



MODE 5

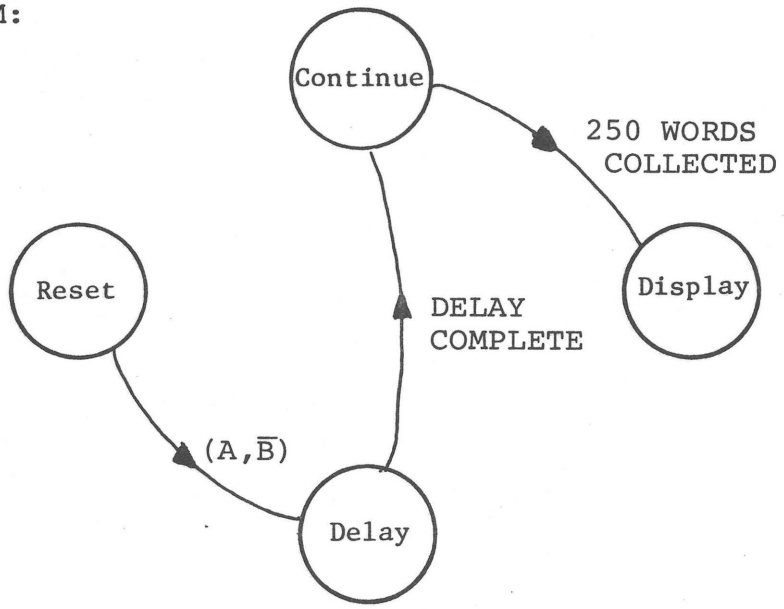
PARALLEL TRIGGER MODE: $(A,\overline{B})$, POS, N CLOCK DELAYS

DESCRIPTION: INITIATE A 250-WORD DATA COLLECTION n CLOCK CYCLES AFTER THE OCCURRENCE OF THE 32-BIT TRIGGER WORD FORMED BY CONCATENATING A WITH ANY WORD OTHER THAN B.

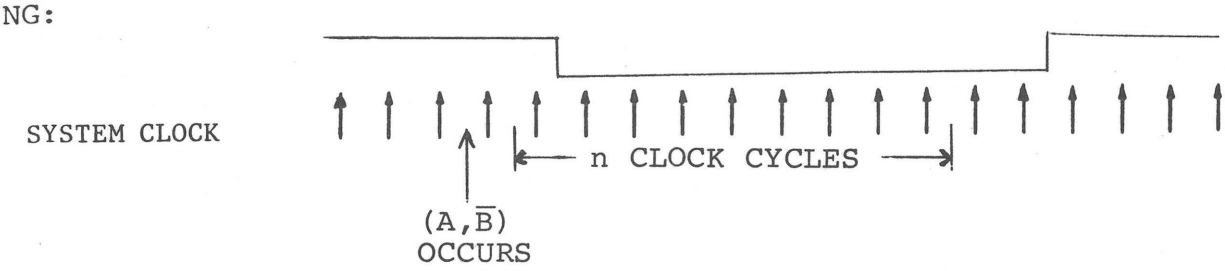
TYPICAL USE: FOR TRIGGERING ON THE OCCURRENCE OF INTERMITTENT OR TRANSIENT DATA. IN THE POSITIVE MODE, THE EFFECTS OF THE TRANSIENT OR ILLEGAL DATA CAN BE TRACED.

DISPLAY: THE FIRST WORD COLLECTED WILL BE THE WORD OCCURRING n CLOCK CYCLES FROM THE TRIGGER WORD A CONCATENATED WITH ANY WORD OTHER THAN $\overline{B}$. THE DELAY OFFSET WILL BE +n AS INDICATED BY TRIGGER LOCATOR AT THE FIRST LINE OF PAGE 0.

STATE DIAGRAM:



TRIG OUTPUT TIMING:



MODE 6

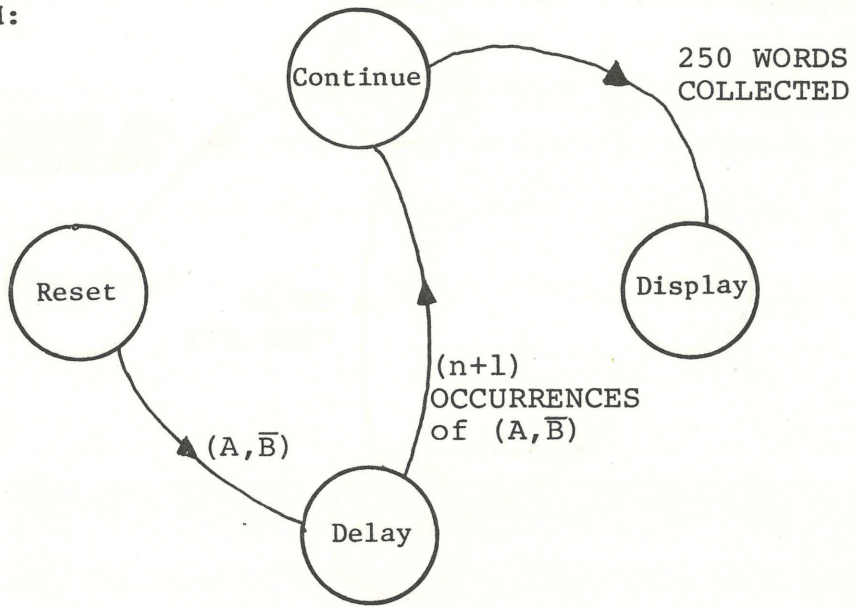
PARALLEL TRIGGER MODE: $(A,\overline{B})$, POS, N TRIG DELAYS

DESCRIPTION: INITIATE A DATA COLLECTION AFTER DELAYING n OCCURRENCES OF THE 32-BIT TRIGGER WORD CONSISTING OF A CONCATENATED WITH ANY WORD OTHER THAN B.

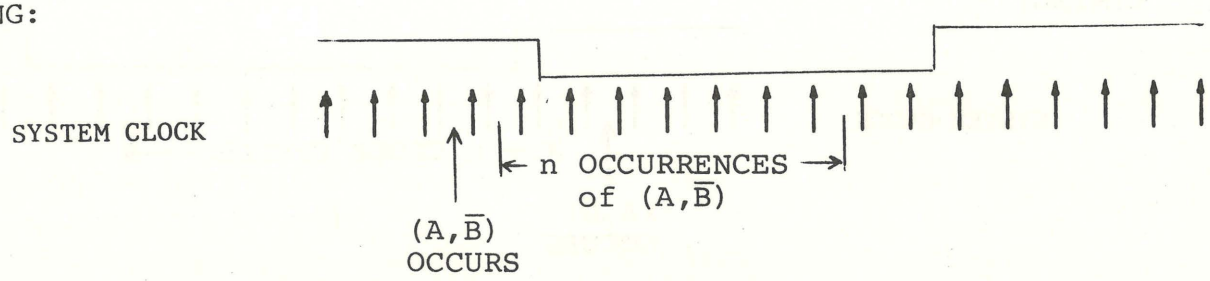
TYPICAL USE: FOR MONITORING A MEMORY LOCATION WHICH IS MODIFIED WITHIN A PROGRAM LOOP AND VIEWING THE n^{th} MODIFICATION.

DISPLAY: THE FIRST WORD WILL BE COLLECTED AT THE $(n+1)^{st}$ OCCURRENCE OF THE TRIGGER WORD A CONCATENATED WITH ANY WORD OTHER THAN B. THE DELAY OFFSET IS $\overline{0}$ AS INDICATED BY "TRIG" AT THE FIRST LINE OF PAGE 0.

STATE DIAGRAM:



TRIG OUTPUT TIMING:



MODE 7

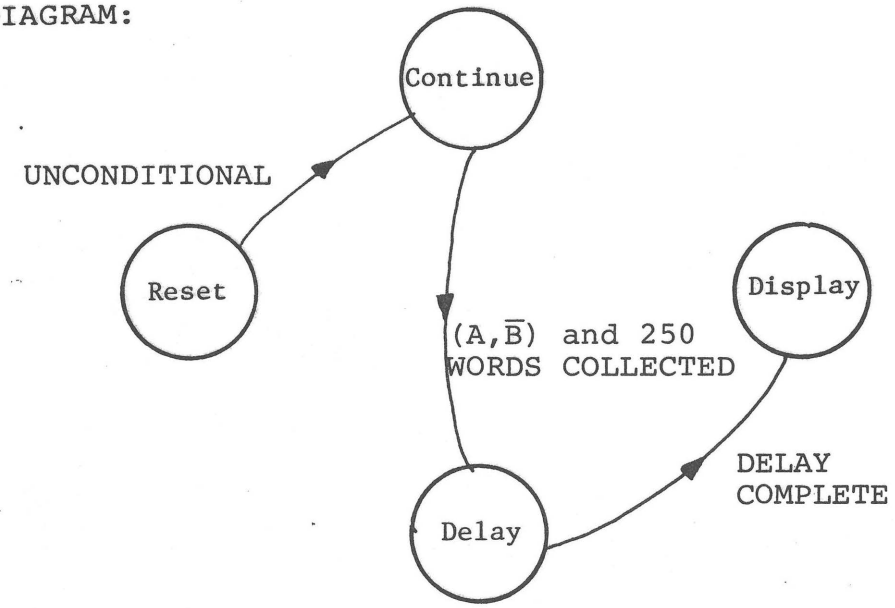
PARALLEL TRIGGER MODE: $(A,\overline{B})$, NEG, N CLOCK DELAYS

DESCRIPTION: HALT DATA COLLECTION n CLOCK CYCLES AFTER OCCURRENCE OF THE 32-BIT TRIGGER WORD FORMED BY CONCATENATING A WITH ANY WORD OTHER THAN B.

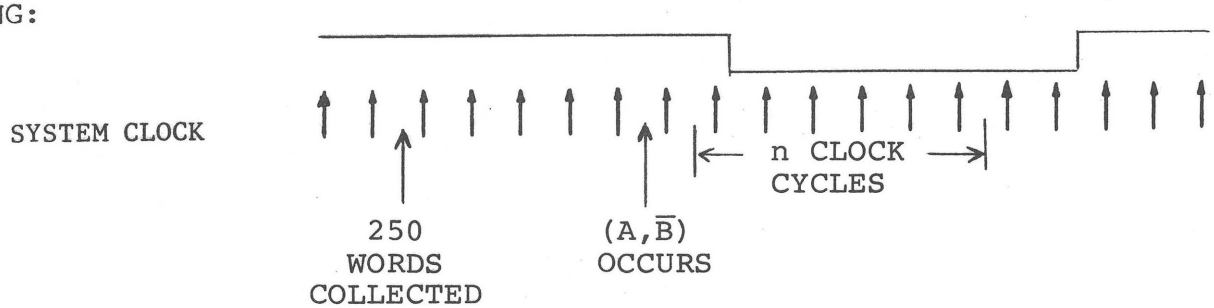
TYPICAL USE: FOR TRIGGERING ON THE ACCESS OF A MEMORY LOCATION THAT CONTAINS INTERMITTENT OR TRANSIENT DATA. IN THE NEGATIVE MODE, THE SEQUENCES LEADING UP TO THE TRANSIENT CONDITION CAN BE TRACED.

DISPLAY: THE LAST WORD COLLECTED IS THE WORD WHICH OCCURS n CLOCK CYCLES FOLLOWING THE TRIGGER WORD A CONCATENATED WITH ANY WORD OTHER THAN B. THE DELAY OFFSET IS +n AS INDICATED BY THE TRIGGER LOCATOR AT THE LAST LINE OF PAGE F.

STATE DIAGRAM:



TRIG OUTPUT
TIMING:



MODE 8

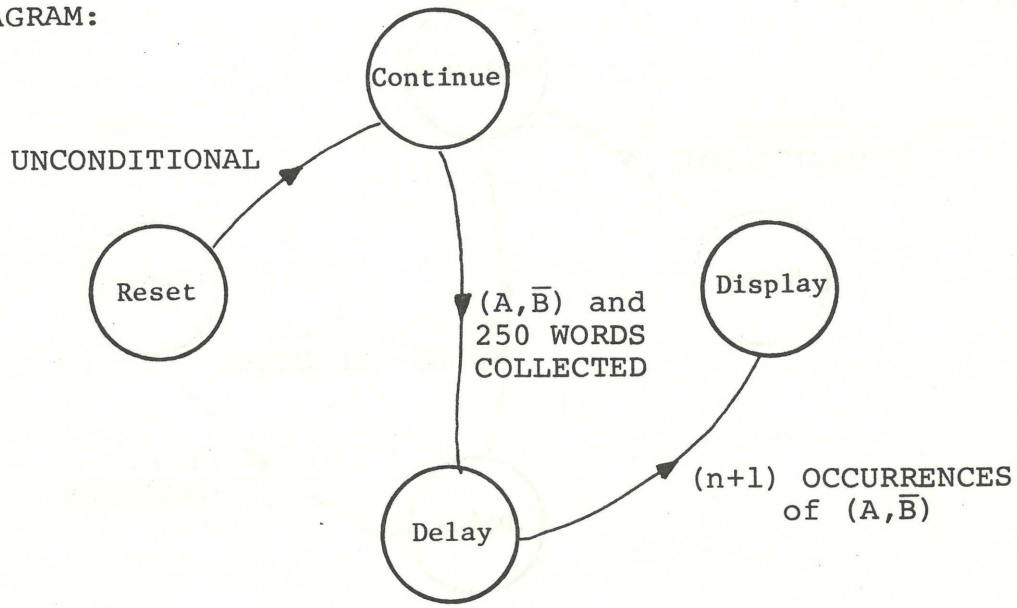
PARALLEL TRIGGER MODE: $(A,\overline{B})$, NEG, N TRIG DELAYS

DESCRIPTION: HALT DATA COLLECTION AFTER DELAYING BY n OCCURRENCES OF THE 32-BIT TRIGGER WORD A CONCATENATED WITH ANY WORD OTHER THAN B.

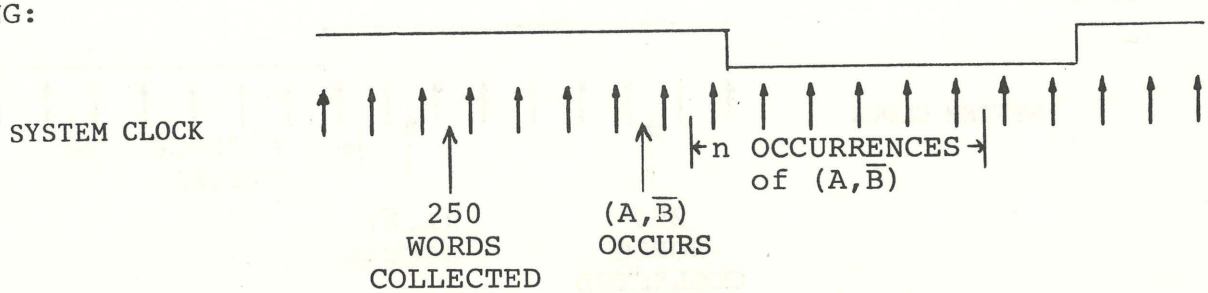
TYPICAL USE: FOR MONITORING A MEMORY LOCATION WHICH IS MODIFIED WITHIN A PROGRAM LOOP AND VIEWING THE ACTIVITY LEADING UP TO THE nTH MODIFICATION.

DISPLAY: THE LAST WORD WILL BE COLLECTED AT THE $(n+1)^{st}$ OCCURRENCE OF THE TRIGGER WORD A CONCATENATED WITH ANY OTHER WORD THAN $\overline{B}$. THE DELAY OFFSET IS 0 AS INDICATED BY "TRIG" AT THE LAST LINE OF PAGE F.

STATE DIAGRAM:



TRIG OUTPUT TIMING:



MODE 9

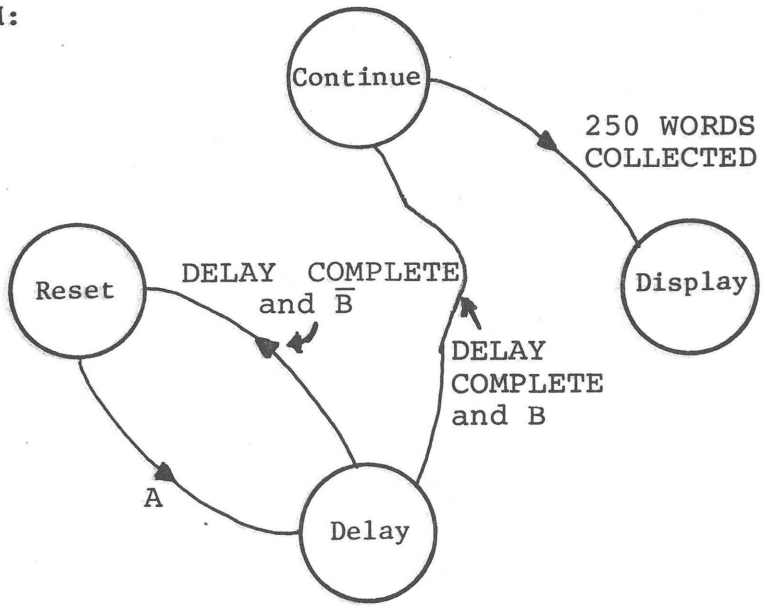
SEQUENTIAL TRIGGER MODE: (A=B), POS, N CLOCK DELAYS

DESCRIPTION: INITIATE A DATA COLLECTION IF B IS EXACTLY n CLOCK CYCLES FROM A. A IS THE FIRST OCCURRENCE OF A 16-BIT WORD IN THE A DATA CHANNEL, B IS THE SECOND OCCURRENCE OF A 16-BIT WORD IN THE A DATA CHANNEL. (B DATA ARE COLLECTED BUT DO NOT AFFECT TRIGGERING.)

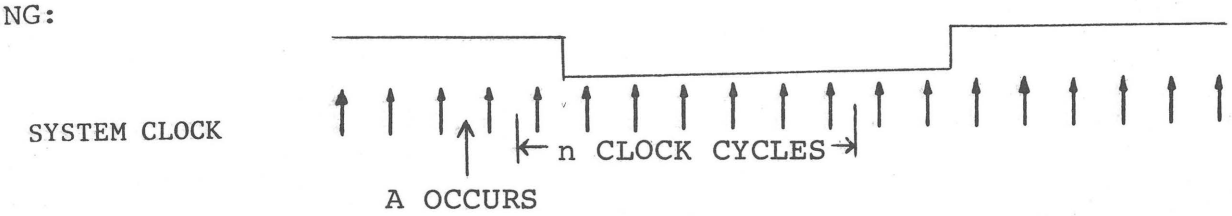
TYPICAL USE: FOR DETERMINING THE SEPARATION BETWEEN TWO ADDRESSES; OR TRIGGERING ONLY WHEN A PARTICULAR ADDRESS SEQUENCE IS ENCOUNTERED. (WHEN SEARCHING FOR THE SEPARATION, THE DELAY COUNT CAN BE SWEPT UNTIL TRIGGERING OCCURS.) FOR PERFORMANCE MONITORING, USE THE TRIG OUTPUT. SET DELAY VALUE TO OFF. SET A=ADDRESS #1; B=ANY VALUE BUT ADDRESS #1. ANALYZER WILL NOT TRIGGER BUT TRIG. OUT WILL BE AT FREQUENCY OF OCCURRENCES OF ADDRESS #1.

DISPLAY: THE FIRST WORD COLLECTED IS THE TRIGGER WORD B WHICH OCCURRED EXACTLY n CYCLES FROM A. THE DELAY OFFSET IS +n AS INDICATED ON THE FIRST LINE OF PAGE 0.

STATE DIAGRAM:



TRIG OUTPUT TIMING:



MODE 10

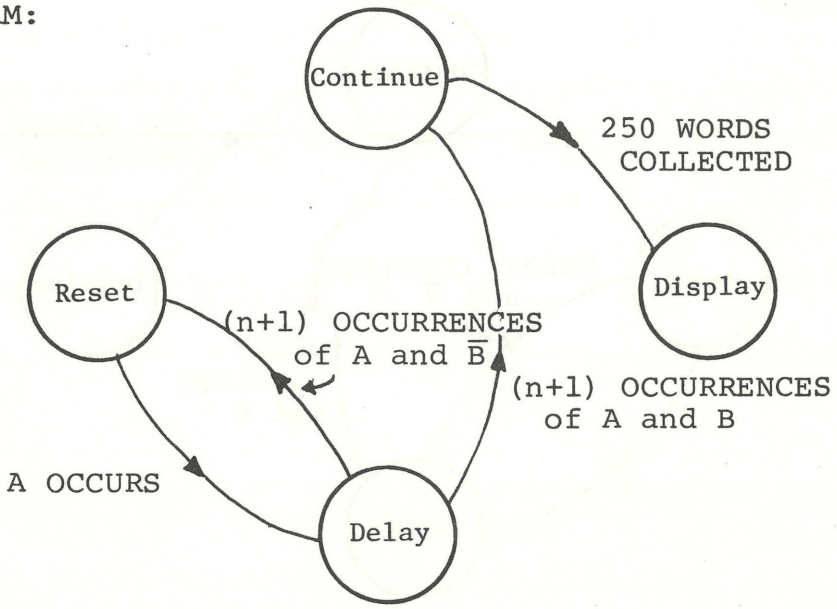
SEQUENTIAL TRIGGER MODE: (A=B), POS, N TRIG DELAYS

DESCRIPTION: INITIATE A DATA COLLECTION IF B IMMEDIATELY FOLLOWS THE $(n+1)^{st}$ OCCURRENCE OF A. A REFERS TO THE FIRST OCCURRENCE OF A 16-BIT WORD IN THE A DATA CHANNEL AND B REFERS TO A SECOND OCCURRENCE OF A 16-BIT WORD IN THE A DATA CHANNEL. (B DATA ARE COLLECTED BUT DO NOT AFFECT TRIGGERING.)

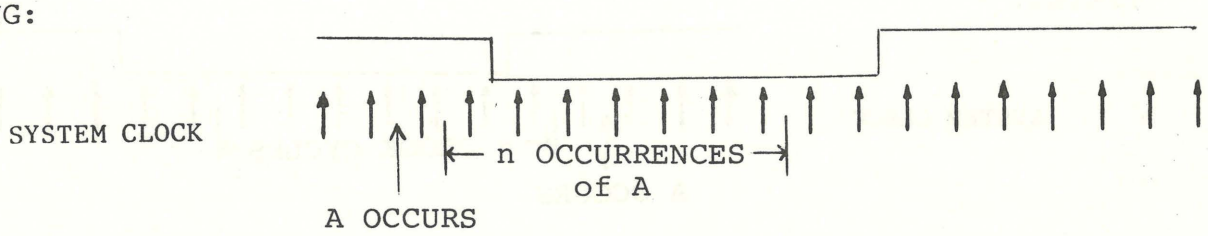
TYPICAL USE: FOR TRIGGERING ON THE n^{th} CALL OF A SUBROUTINE. A IS THE CALL ADDRESS IN THE MAIN PROGRAM AND B IS THE SUBROUTINE ADDRESS.

DISPLAY: THE FIRST WORD WILL BE COLLECTED IN THE A DATA CHANNEL AT THE $(n+1)^{st}$ OCCURRENCE OF THE TRIGGER WORD A. THE SECOND WORD COLLECTED IN THE A DATA CHANNEL IS B. THE DELAY OFFSET IS 0 AS INDICATED BY "TRIG" AT THE FIRST LINE OF PAGE 0.

STATE DIAGRAM:



TRIG OUTPUT TIMING:



MODE 11

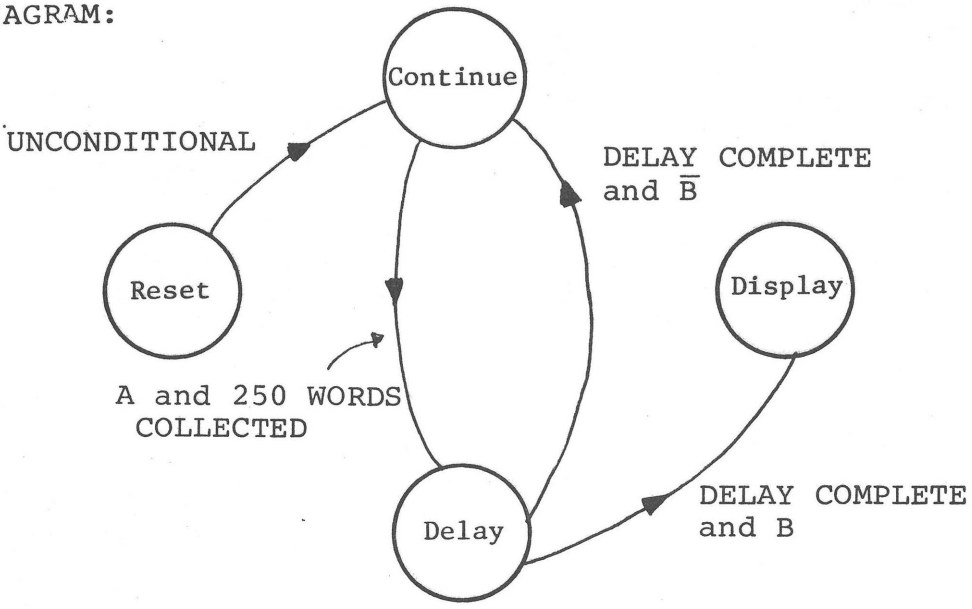
SEQUENTIAL TRIGGERING MODE: (A=B), NEG, N CLOCK DELAYS

DESCRIPTION: HALT DATA COLLECTION IF B FOLLOWS A BY EXACTLY n CLOCK CYCLES. A IS THE FIRST OCCURRENCE OF A 16-BIT WORD IN THE A DATA CHANNEL; B IS THE SECOND OCCURRENCE OF A 16-BIT WORD IN THE A DATA CHANNEL. B DATA ARE COLLECTED BUT DO NOT AFFECT TRIGGERING.

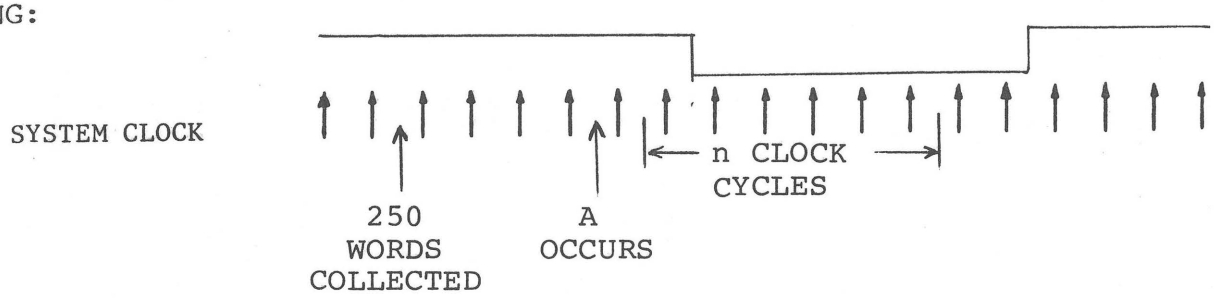
TYPICAL USE: FOR TRIGGERING ONLY WHEN A PARTICULAR ADDRESS SEQUENCE IS ENCOUNTERED. THE NEGATIVE MODE ALLOWS VIEWING ACTIVITY LEADING UP TO THE PARTICULAR SEQUENCE.

DISPLAY: THE LAST WORD COLLECTED IS THE TRIGGER WORD B WHICH OCCURRED EXACTLY n CLOCK CYCLES FROM A. IF n IS ≤ 249, A WILL BE CONTAINED IN THIS DATA COLLECTION. THE DELAY OFFSET IS +n AS INDICATED BY THE TRIGGER LOCATOR AT THE LAST LINE IN PAGE F.

STATE DIAGRAM:



TRIG OUTPUT
TIMING:



MODE 12

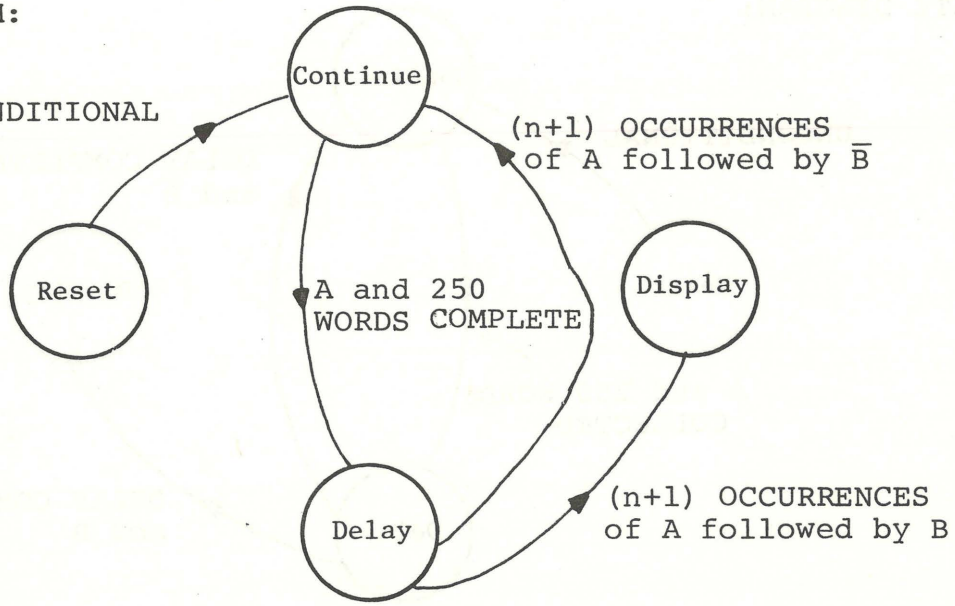
SEQUENTIAL TRIGGERING MODE: (A=B), NEG, N TRIG DELAYS

DESCRIPTION: HALT DATA COLLECTION IF B IMMEDIATELY FOLLOWS THE $(n+1)^{st}$ OCCURRENCE OF A. A IS THE FIRST OCCURRENCE OF A 16-BIT WORD IN A DATA CHANNEL AND B IS THE SECOND OCCURRENCE OF A 16-BIT WORD IN THE A DATA CHANNEL. B DATA ARE COLLECTED BUT DO NOT AFFECT TRIGGERING.

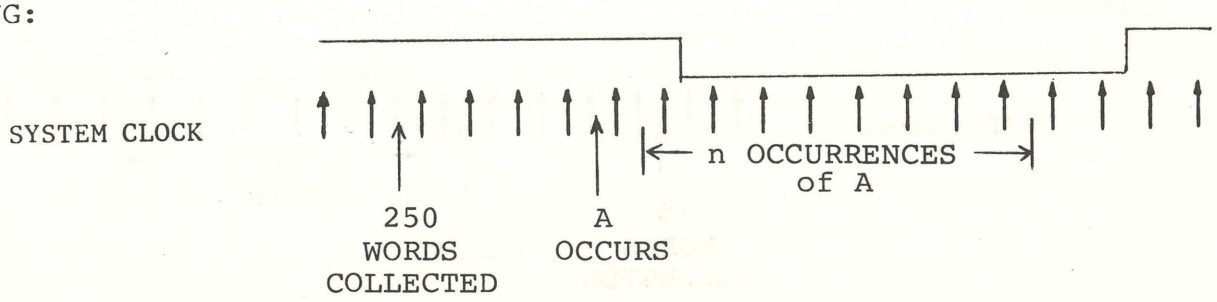
TYPICAL USE: FOR ANALYSIS OF COMPUTER PROGRAMS WHERE A COMMON CODE BLOCK IS USED BY SEVERAL DIFFERENT MAIN LINE PROGRAMS. FOR EXAMPLE, IF A IS A SUBROUTINE EXIT ADDRESS AND B IS THE RETURN ADDRESS OF THE MAIN PROGRAM, THIS MODE PERMITS ANALYZING THE $(n+1)^{st}$ CALL OF A BY THE MAIN PROGRAM B. PRE-TRIGGERING PERMITS ANALYSIS OF ACTIVITY PRECEDING B.

DISPLAY: THE LAST WORD WILL BE COLLECTED AT THE $(n+1)^{st}$ OCCURRENCE OF THE TRIGGER WORD A WHICH WAS IMMEDIATELY FOLLOWED BY B.

STATE DIAGRAM:



TRIG OUTPUT TIMING:



MODE 13

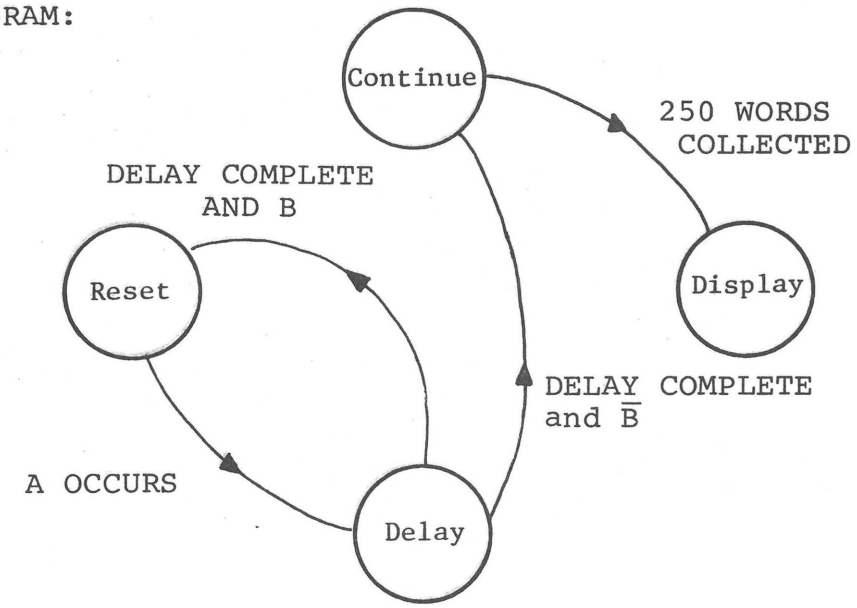
SEQUENTIAL TRIGGERING MODE: (A=$\overline{B}$), POS, N CLOCK DELAYS

DESCRIPTION: INITIATE A DATA COLLECTION IF ANYTHING BUT B FOLLOWS A BY EXACTLY n CLOCK CYCLES. A IS THE FIRST OCCURRENCE OF A 16-BIT TRIGGER WORD IN THE A DATA CHANNEL, B IS THE SECOND OCCURRENCE OF A 16-BIT WORD IN THE A DATA CHANNEL. B DATA ARE COLLECTED BUT DO NOT AFFECT TRIGGERING.

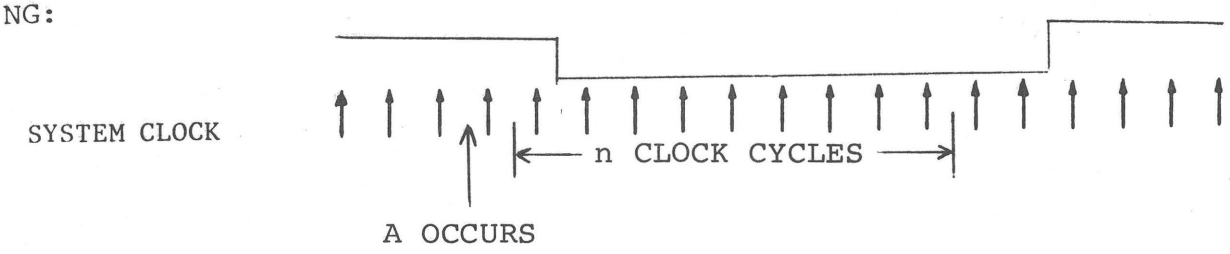
TYPICAL USE: ANALYSIS OF AN ILLEGAL PROGRAM SEQUENCE OR TRANSIENT ERROR. THE EXPECTED SEQUENCE IS SET INTO THE ANALYZER. WHEN THIS SEQUENCE DOES NOT OCCUR, THE ANALYZER TRIGGERS AND COLLECTS DATA. THIS MODE IS USEFUL FOR ANALYSIS OF INTERMITTENTLY OCCURRING HARDWARE OR SOFTWARE FAULTS.

DISPLAY: THE FIRST WORD COLLECTED WILL BE THE DATA WHICH OCCURRED EXACTLY n CLOCK CYCLES FROM A. THIS DATA CAN BE ANYTHING BUT B. THE DELAY OFFSET IS +n AS INDICATED BY THE TRIGGER LOCATOR AT THE FIRST LINE OF PAGE 0.

STATE DIAGRAM:



TRIG OUTPUT TIMING:



MODE 14

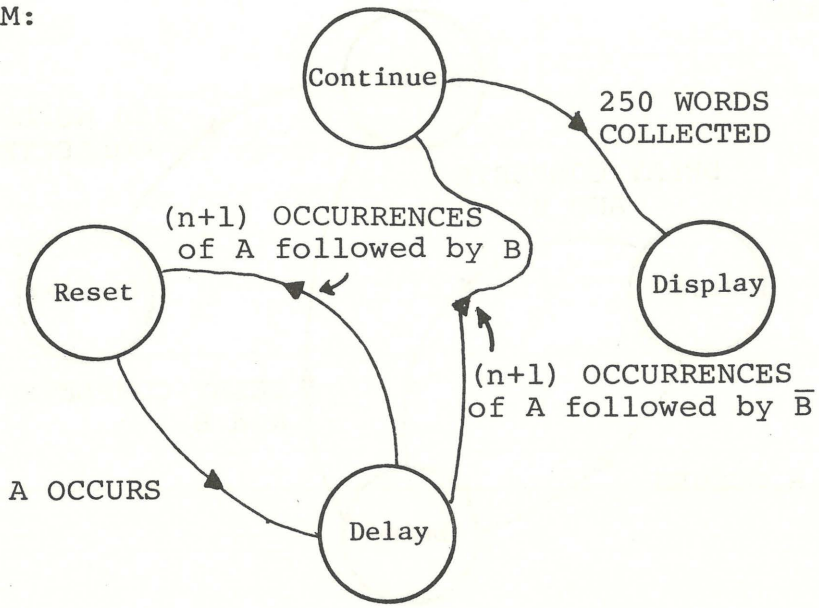
SEQUENTIAL TRIGGERING MODE: $(A=\overline{B})$, POS, N TRIG DELAYS

DESCRIPTION: INITIATE A DATA COLLECTION IF B DOES NOT IMMEDIATELY FOLLOW THE $(n+1)^{st}$ OCCURRENCES OF A. A IS THE FIRST OCCURRENCE OF A 16-BIT TRIGGER WORD IN THE A DATA CHANNEL; B IS THE SECOND OCCURRENCE OF A 16-BIT WORD IN THE A DATA CHANNEL. B DATA ARE COLLECTED BUT DO NOT AFFECT TRIGGERING.

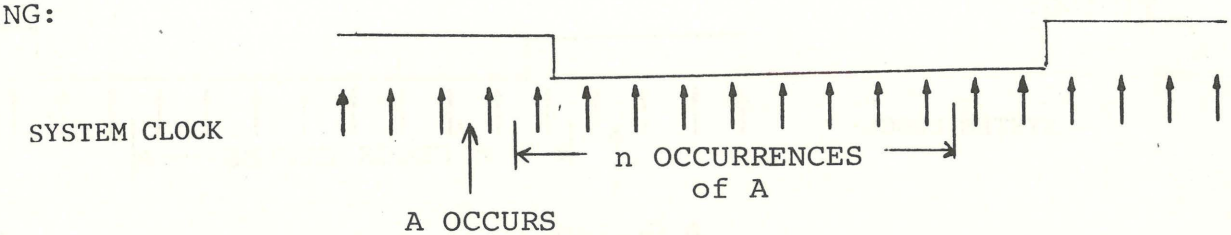
TYPICAL USE: FOR USE IN THE ANALYSIS OF SOFTWARE AND HARDWARE-CONTROLLED TIGHT LOOPS. FOR EXAMPLE, A COULD BE THE MICROPROGRAM ADDRESS FOR THE MULTIPLY ITERATION LOOP IN A MICROPROGRAMMED MACHINE. B COULD THEN BE SET TO MONITOR THE VARIOUS ESCAPE ADDRESSES.

DISPLAY: THE FIRST WORD WILL BE COLLECTED AT THE $(n+1)^{st}$ OCCURRENCE OF A. THE DELAY OFFSET IS 0 AS INDICATED BY THE LABEL "TRIG" ON LINE 1 OF PAGE 0.

STATE DIAGRAM:



TRIG OUTPUT TIMING:



MODE 15

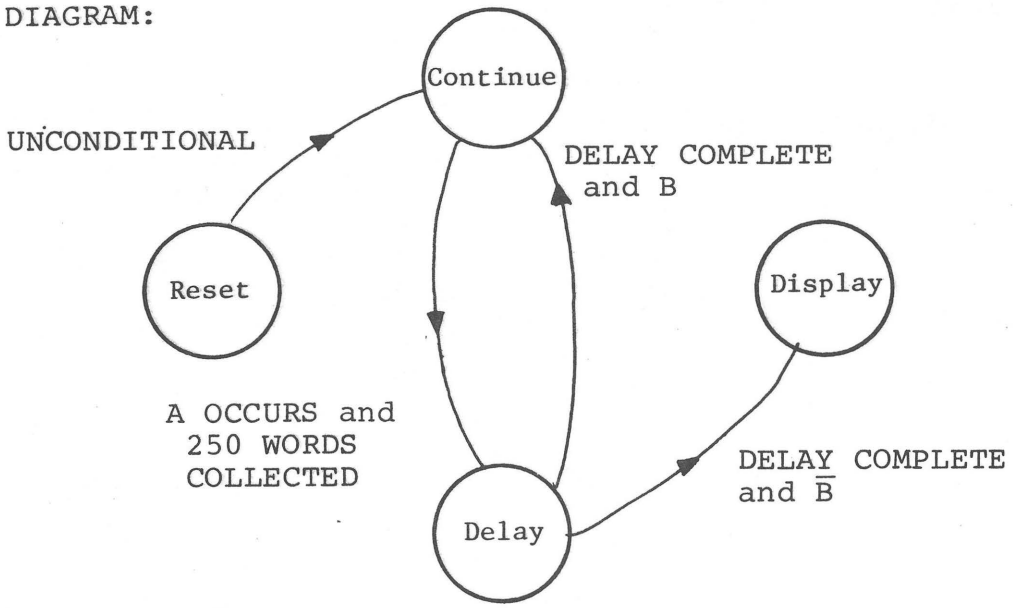
SEQUENTIAL TRIGGERING MODE: (A=$\overline{B}$), NEG, N CLOCK DELAYS

DESCRIPTION: HALT DATA COLLECTION IF ANYTHING BUT $\overline{B}$ FOLLOWS A BY EXACTLY n CLOCK CYCLES. A IS THE FIRST OCCURRENCE OF A 16-BIT TRIGGER WORD IN THE A DATA CHANNEL; B IS THE SECOND OCCURRENCE OF A 16-BIT WORD IN THE A DATA CHANNEL. B DATA ARE COLLECTED BUT DO NOT AFFECT TRIGGERING.

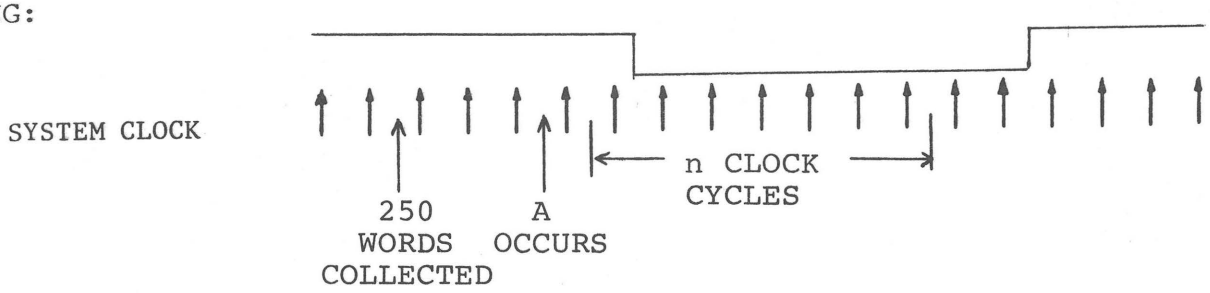
TYPICAL USE: FOR ANALYSIS OF AN ILLEGAL PROGRAM SEQUENCE OR A TRANSIENT ERROR. WHEN THE EXPECTED SEQUENCE DOES NOT OCCUR, THE ACTIVITY LEADING UP TO THE SEQUENCE CAN BE OBSERVED.

DISPLAY: THE LAST WORD COLLECTED CONTAINS THE DATA WHICH OCCURRED EXACTLY n CLOCK CYCLES FROM A. THIS DATA WILL BE DIFFERENT FROM $\overline{B}$. THE DELAY OFFSET IS ±n AS INDICATED BY THE TRIGGER LOCATOR AT THE LAST LINE OF PAGE F.

STATE DIAGRAM:



TRIG OUTPUT
TIMING:



MODE 16

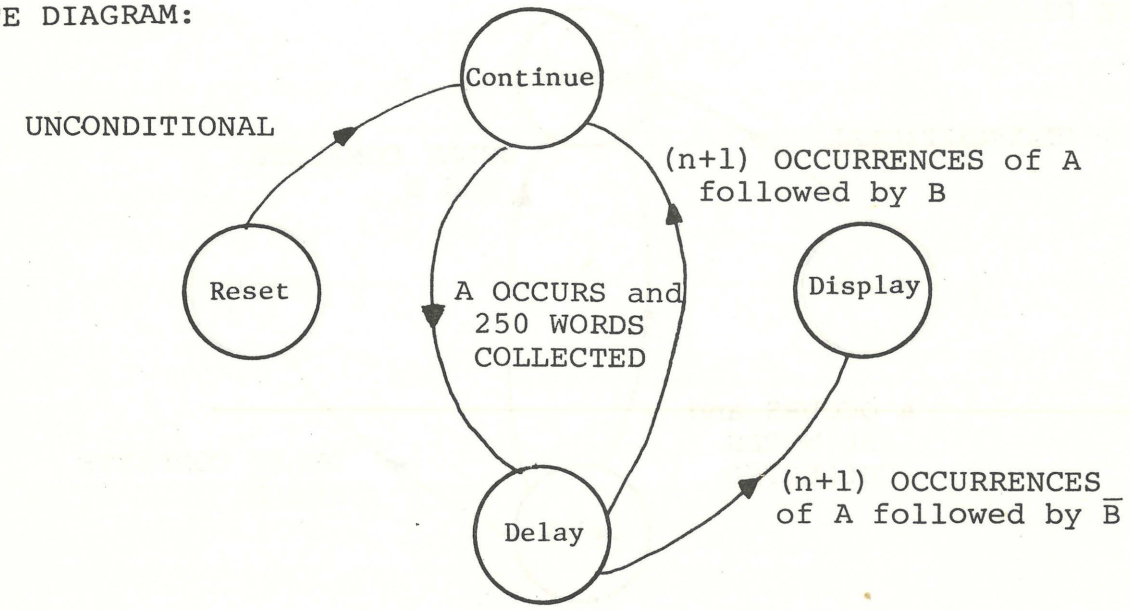
SEQUENTIAL TRIGGERING MODE: (A=B), NEG, N TRIG DELAYS

DESCRIPTION: HALT DATA COLLECTION IF $\overline{B}$ DOES NOT IMMEDIATELY FOLLOW THE (n+1)st OCCURRENCE OF A. A IS THE FIRST OCCURRENCE OF A 16-BIT TRIGGER WORD IN THE A DATA CHANNEL; B IS THE SECOND OCCURRENCE OF A 16-BIT WORD IN THE A DATA CHANNEL. B DATA ARE COLLECTED BUT DO NOT AFFECT TRIGGERING.

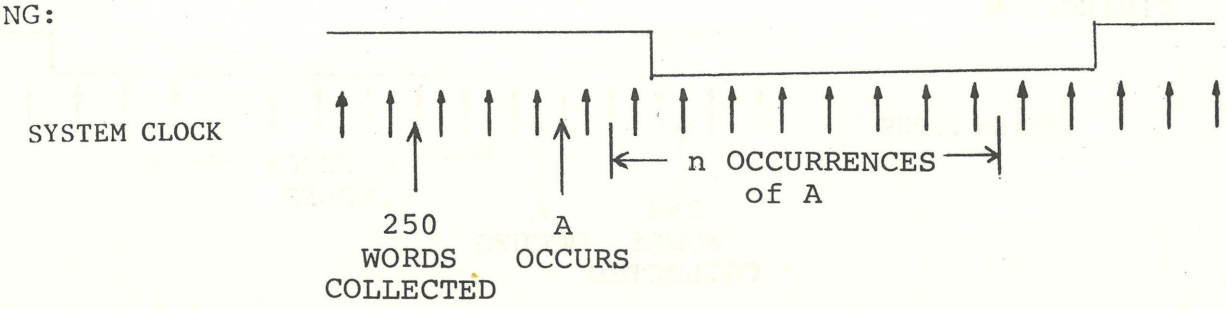
TYPICAL USE: FOR USE IN THE ANALYSIS OF SOFTWARE OR HARDWARE CONTROLLED TIGHT LOOPS. ACTIVITY LEADING UP TO THE TIGHT LOOP EXIT CAN BE ANALYZED IN THE NEGATIVE MODE.

DISPLAY: THE LAST WORD WILL BE COLLECTED AT ANY (n+1)st OCCURRENCE OF A, WHICH WAS IMMEDIATELY FOLLOWED BY ANY EVENT OTHER THAN B. THE DELAY OFFSET IS 0 AS INDICATED BY THE LABEL "TRIG" AT THE LAST LINE OF PAGE F.

STATE DIAGRAM:



TRIG OUTPUT TIMING:



MODE 17

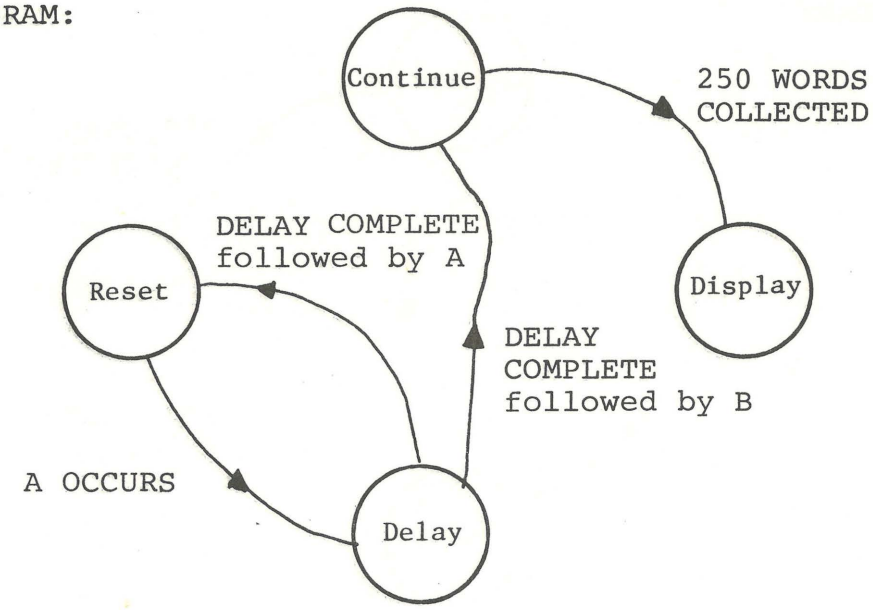
SEQUENTIAL TRIGGERING MODE: (A≥B), POS, N CLOCK DELAYS

DESCRIPTION: INITIATE A DATA COLLECTION IF B OCCURS AT LEAST n CLOCK CYCLES FROM A. A IS THE FIRST OCCURRENCE OF A 16-BIT WORD IN THE A DATA CHANNEL; B IS THE SECOND OCCURRENCE OF A 16-BIT WORD IN THE A DATA CHANNEL. IF, AFTER THE DELAY IS COMPLETE, A OCCURS AGAIN BEFORE B, THE RESET STATE IS ENTERED AND THE ANALYZER WAITS FOR ANOTHER A FOLLOWED BY B SEQUENCE. B DATA ARE COLLECTED BUT DO NOT AFFECT TRIGGERING.

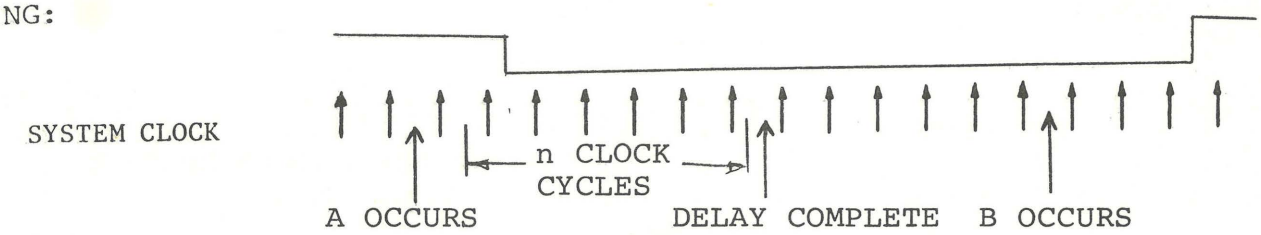
TYPICAL USE: ANALYSIS OF COMPUTER PROGRAM FLOW BY ARMING ON THE FIRST ADDRESS AND HOLDING OFF COLLECTION FOR A NUMBER OF CLOCK CYCLES. FOR EXAMPLE, THIS MODE CAN BE USED TO ANALYZE A PASS THROUGH A SUB-ROUTINE LOOP THAT CONTAINS AN ADDRESS B WHICH IS CALLED FROM LOCATION A. SINCE EXACT EQUALITY ON THE DELAY NEED NOT BE MET, THIS MODE CAN HANDLE VARIATIONS IN PROGRAM CYCLE LENGTH. FOR PERFORMANCE MONITORING, THE TRIG OUTPUT CAN BE USED. SET A = ADDRESS #1, SET B = ADDRESS #2, SET CLOCK DLY = 0001. TRIG OUTPUT IS LOW DURING TIME BETWEEN A AND B AND CAN BE USED TO GATE AN INTERVAL COUNTER.

DISPLAY: THE FIRST WORD COLLECTED WILL BE THE TRIGGER WORD B WHICH OCCURRED AT LEAST n CLOCK CYCLES FROM A. THE DELAY OFFSET IS 0 AS INDICATED BY THE LABEL "TRIG" AT THE FIRST LINE ON PAGE 0.

STATE DIAGRAM:



TRIG OUTPUT TIMING:



MODE 18

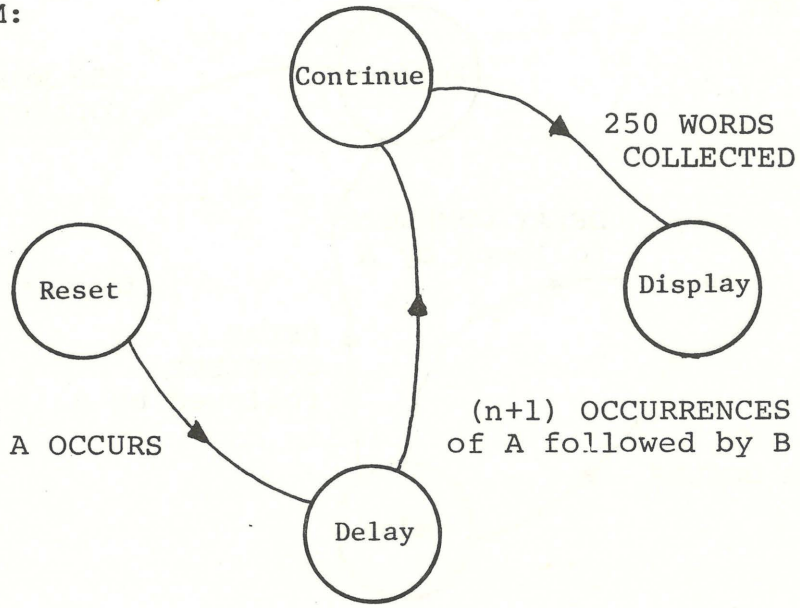
SEQUENTIAL TRIGGERING MODE: (A≥B), POS, N TRIG DELAYS

DESCRIPTION: INITIATE A DATA COLLECTION IF B OCCURS ANYTIME AFTER THE (n+1)st OCCURRENCE OF A. A IS THE FIRST OCCURRENCE OF A 16-BIT TRIGGER WORD IN THE A DATA CHANNEL; B IS THE SECOND OCCURRENCE OF A TRIGGER WORD IN THE A CHANNEL. B DATA ARE COLLECTED BUT DO NOT AFFECT TRIGGERING.

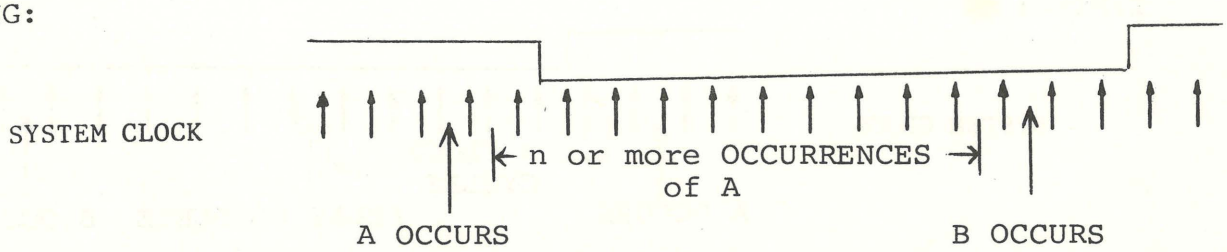
TYPICAL USE: FOR USE IN PROGRAM LOOP ANALYSIS WHERE THE OCCURRENCE OF ADDRESS B IS PREDICATED ON (n+1) OCCURRENCES OF A. FOR EXAMPLE, ALLOWING THE TRIGGERING OF THE ANALYZER ONLY AFTER A SUBROUTINE HAS BEEN CALLED A NUMBER OF TIMES.

DISPLAY: THE FIRST WORD COLLECTED REPRESENTS THE FIRST TIME TRIGGER WORD B IS FOLLOWED BY AT LEAST (n+1) OCCURRENCES OF A. THE DELAY OFFSET VALUE IS 0 AS INDICATED BY THE LABEL "TRIG" AT THE FIRST LINE OF PAGE 0.

STATE DIAGRAM:



TRIG OUTPUT TIMING:



MODE 19

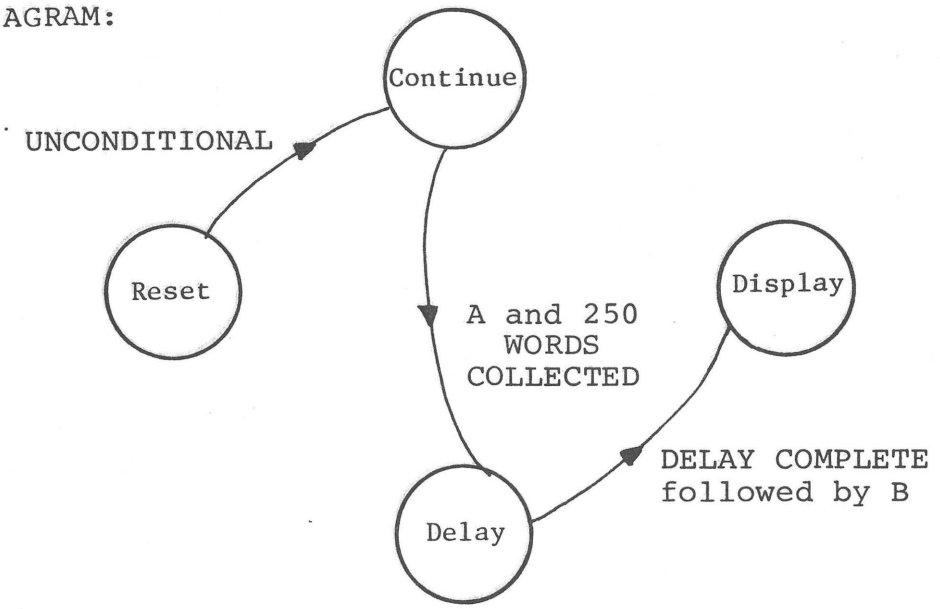
SEQUENTIAL TRIGGERING MODE: (A≥B), NEG, N CLOCK DELAYS

DESCRIPTION: HALT DATA COLLECTION IF B OCCURS AT LEAST n CLOCK PULSES FROM A. A IS THE FIRST OCCURRENCE OF A 16-BIT TRIGGER WORD IN THE A DATA CHANNEL; B IS THE SECOND OCCURRENCE OF A 16-BIT TRIGGER WORD IN THE A DATA CHANNEL. IF, AFTER THE DELAY IS COMPLETE, A OCCURS BEFORE B, THE ANALYZER IS RESET AND WAITS FOR ANOTHER SEQUENCE WHERE A IS FOLLOWED BY B. B DATA ARE COLLECTED BUT DO NOT AFFECT TRIGGERING.

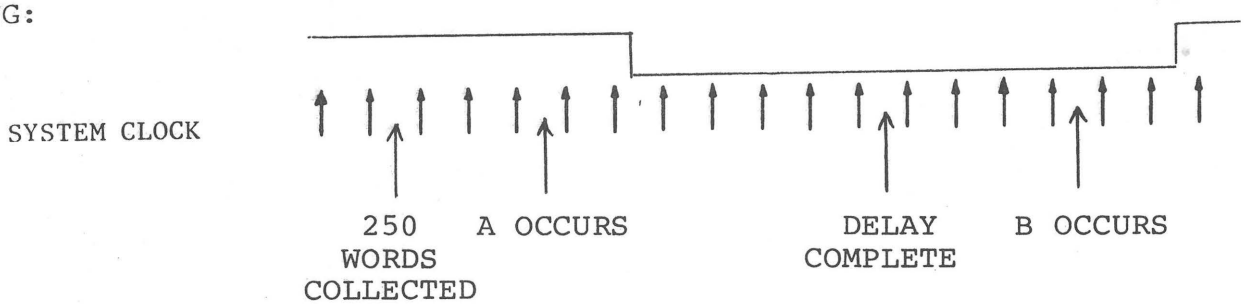
TYPICAL USE: FOR ANALYSIS OF COMPUTER PROGRAM FLOW BY ARMING ON THE FIRST ADDRESS BUT HOLDING DATA COLLECTION OFF A NUMBER OF CLOCK CYCLES BEFORE A SECOND ADDRESS IS RECOGNIZED. IN THE NEGATIVE MODE, THE ACTIVITY PRECEDING THE SECOND ADDRESS CAN BE ANALYZED.

DISPLAY: THE LAST WORD COLLECTED CONTAINS THE TRIGGER WORD B WHICH OCCURRED AT LEAST n CLOCK CYCLES AFTER A. THE DELAY OFFSET IS 0 AS INDICATED BY THE LABEL "TRIG" AT THE LAST LINE OF PAGE F.

STATE DIAGRAM:



TRIG OUTPUT
TIMING:



MODE 20

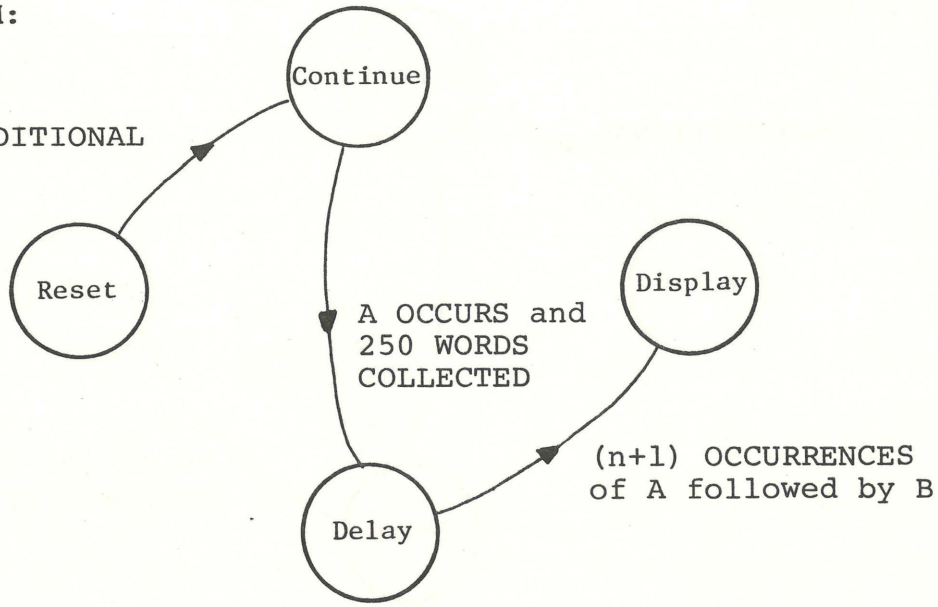
SEQUENTIAL TRIGGERING MODE: (A≥B), NEG, N TRIG DELAYS

DESCRIPTION: HALT DATA COLLECTION IF B OCCURS ANYTIME AFTER (n+1) OCCURRENCES OF A. A IS THE FIRST OCCURRENCE OF A 16-BIT TRIGGER WORD IN THE A DATA CHANNEL; B IS THE SECOND OCCURRENCE OF A TRIGGER WORD IN THE A DATA CHANNEL. B DATA ARE COLLECTED BUT DO NOT AFFECT TRIGGERING.

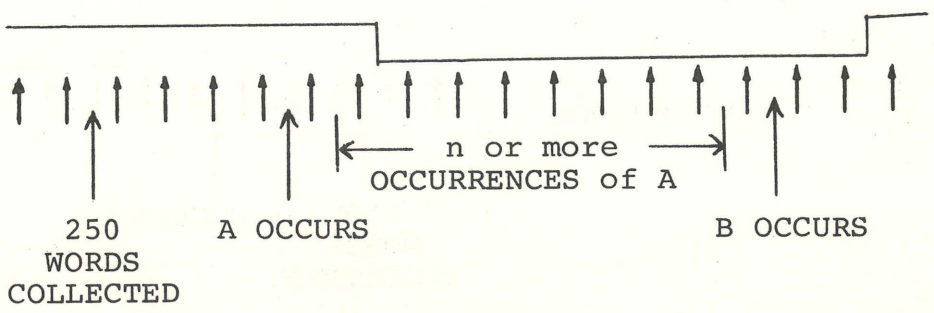
TYPICAL USE: USED IN PROGRAM LOOP ANALYSIS WHERE THE OCCURRENCE OF AN ADDRESS B IS PREDICATED ON (n+1) OCCURRENCES OF A. IN THE NEGATIVE MODE, ACTIVITY LEADING UP TO B CAN BE ANALYZED.

DISPLAY: THE LAST WORD COLLECTED IS THE FIRST OCCURRENCE OF TRIGGER WORD B WHICH IS PRECEDED BY AT LEAST (n+1) OCCURRENCES OF A. THE DELAY OFFSET VALUE IS 0 AS INDICATED BY THE LABEL "TRIG" AT THE LAST LINE OF PAGE F.

STATE DIAGRAM:



TRIG OUTPUT TIMING:



MODE 21

SEQUENTIAL TRIGGER MODE: STOP A/STOP B, DELAY = OFF

DESCRIPTION: START DATA COLLECTION ON THE OCCURRENCE OF A; STOP COLLECTION ON THE OCCURRENCE OF B. IF MORE THAN 250 CLOCK CYCLES SEPARATE A AND B, ONLY THE MOST RECENT 250 ARE RETAINED. A IS THE FIRST OCCURRENCE OF A 16-BIT TRIGGER WORD IN THE A DATA CHANNEL; B IS THE SECOND OCCURRENCE OF A 16-BIT TRIGGER WORD IN THE A DATA CHANNEL. B DATA ARE COLLECTED BUT DO NOT AFFECT TRIGGERING. SIGNATURES ARE CALCULATED ONLY ON THE AMOUNT OF DATA ACTUALLY COLLECTED.

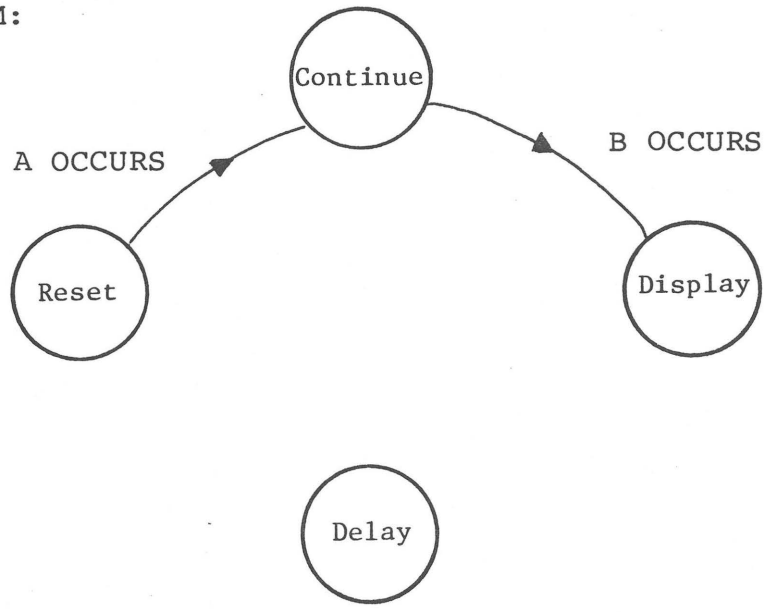
TYPICAL USE: FOR USE IN CONTROLLING THE NUMBER OF WORDS COLLECTED. THIS PERMITS SIGNATURE COMPARISONS ON ANY SELECTED CODE BLOCK UP TO 250 CYCLES IN LENGTH. NOTE THAT THE DATA ACQUISITION TIME WILL BE REDUCED IN PROPORTION TO THE NUMBER OF WORDS COLLECTED.

DISPLAY:

CASE 1-THE SEPARATION BETWEEN A AND B IS $\leq$ 250 CLOCK CYCLES: THE FIRST WORD COLLECTED IS THE TRIGGER WORD A. THE LAST WORD COLLECTED--WHICH MAY NOT BE ON PAGE F--IS THE TRIGGER WORD B. THE SIGNATURE IS COMPUTED ONLY ON THE ACTIVE WORDS COLLECTED.

CASE 2-THE SEPARATION BETWEEN A AND B IS $>$ 250 CLOCK CYCLES: THE FIRST WORD COLLECTED IS THE ONE WHICH PRECEDED B BY 249 CLOCK CYCLES; THE LAST WORD COLLECTED IS THE TRIGGER WORD B. NOTE THAT THE SIGNATURE IS COMPUTED ON ALL 250 WORDS.

STATE DIAGRAM:



TRIG OUTPUT TIMING: NOT ACTIVATED IN THIS MODE

9.0 TYPICAL LOGIC STATE ANALYSIS APPLICATIONS

As described in Section 1.0, the Model 532 has the electrical and mechanical features required to support R&D, field service, and production test applications. In this section, examples of typical Model 532 applications in those areas are presented. These applications are designed to illustrate the power of the instrument and may suggest additional analysis approaches which relate to the user's problem at hand.

9.1 R & D APPLICATIONS

For R&D, the suggested minimum configuration of the instrument is the Model 532B (12 MHz), two Model 51 (variable threshold) probes, and the Auxiliary Memory Board.

With this configuration, the development engineer can:

1. Choose from among 21 powerful triggering modes.
2. Utilize the 32-bit-wide, 250-word-deep trace memory.
3. Collect data at a basic system clock rate of 12 MHz.
4. Store data collections in the Auxiliary Memory for later comparison.
5. Interface with all major logic families with minimum loading.
6. Take advantage of a 32-bit-wide trigger word plus 4 qualifiers.

9.1.1 DEVELOPMENT AND CHECKOUT OF A MICROPROGRAMMED COMPUTER

One of the most challenging applications for a logic state analyzer in the lab is in support of the development and checkout of a high-speed microprogrammed computer. Assume, by way of example, that a 16-bit machine is under development and consists of four 4-bit bipolar slices (such as the AMD 2901), plus the microprogram memory, microsequencer, and

other logic. Assume, also, that the microprogram is in a tight loop which is monitoring an external control panel input. However, when this input is activated, it appears that the correct microsequence is never entered. The problem is to find out where the tight loop exits when the control panel is activated.

From the nature of the problem, the following test setup is suggested:

MODEL 532	SYSTEM-UNDER-TEST
A DATA CHANNEL	Microprogram address bus (usually 8-12 bits), plus microsequencer status inputs (usually 4-8 bits)
A CLOCK	Microcycle clock
B DATA CHANNEL	CPU output bus (16 bits)
B CLOCK	Set for A CLOCK

With this test setup, the Model 532 would be configured to trigger as follows:

A TRIGGER WORD	Address of loop
B TRIGGER WORD	Address of loop
CLOCK DELAY	0001
TRIGGER MODE	(A=$\overline{B}$), POS
DISPLAY/HOLD CONTROL	HOLD

The use of the ($A=\overline{B}$) mode guarantees that the analyzer will not trigger as long as the microprogram is in the tight monitoring loop. However, when the control panel input is activated and the loop is exited, the Model 532 will trigger and collect and display the resulting incorrect microsequence for detailed analysis. Although the user could examine the microsequence line-by-line using the Model 532's WORD mode, it would be more convenient and faster to use the instrument with an ordinary lab scope and examine the collected data in 16-word pages.

9.2 FIELD SERVICE APPLICATIONS

In field service, the primary functions of a logic state analyzer are to minimize customer down-time and to reduce the "floating inventory" costs associated with board swapping. Toward these ends, a suggested minimum configuration of the instrument is the Model 532B (12 MHz), two Model 50 (fixed TTL threshold) probes, an Auxiliary Memory Board, and a Serial Interface Board (SIB). (A scope is not essential.)

With this configuration, the field engineer (FE) can:

1. Perform both GO/NO-GO testing and detailed fault isolation.
2. Call upon the testing and analysis resources of the factory or central field service office using an ordinary modem and a telephone line.
3. Capture and display intermittent failures using the analyzer's HOLD $\neq$ mode.

9.2.1 FIELD SERVICE OF A PLANT PROCESS CONTROLLER

Assume that the FE is called in to repair a troublesome microprocessor- or minicomputer-based plant process controller. In order to minimize repeated service calls, it is desirable for the FE to ascertain the overall status of the system during his first call. The use of maintenance ports

(as described in Section 7.0) and/or Model 52 terminators with pre-configured IC clips will greatly speed up system interconnection and the analysis of critical signals.

The following test setup is suggested for debugging the process controller:

MODEL 532	SYSTEM-UNDER-TEST
A DATA CHANNEL	Controller address bus.
B DATA CHANNEL	I/O, ports, sensor and actuator interfaces, and other critical signals.

The FE can perform a general status check by exercising the controller while performing standard tests previously stored in the auxiliary memory. Any discrepancies between actual and expected test results will be evident from flashing signatures. Fault isolation will be aided by an examination of the contents of the data memory for the word or words responsible for the fault; these will be flashing as well.

If additional testing is required, the FE can access the resources at the factory or central field service office by having these additional tests downloaded via a telephone line and a modem. The Model 532 will automatically execute these tests and send the results back to the central office for detailed analysis. If the problem is determined to be intermittent, i.e., the controller "crashes" once a day, the Model 532 can be used in the HOLD $\neq$ mode. In this mode, performance of the subsystem in questions would be continually monitored and checked for proper operation by the analyzer. The FE could then leave to make other calls. As soon as the anomaly occurred, the analyzer would capture the events surrounding the "crash" and retain the evidence until the FE returned.

This "babysitting" mode of the Model 532 is extremely powerful since it permits the FE to perform other service duties. Also, many intermittent failures cannot be confidently repaired by board swapping due to the uncertainties associated with both the fault and its time of occurrence.

9.3 PRODUCTION TEST APPLICATIONS

For production test, a suggested minimum configuration of the instrument is the Model 532A (5 MHz), two Model 50 (fixed TTL threshold) probes, the Auxiliary Memory Board, and the Serial (RS-232C/TTY) or Parallel (IEEE-488) Interface Board.

With this configuration, the operator can:

1. Monitor 32 critical signals and capture 250 words at a time.
2. Utilize automatic testing with GO/NO-GO indications.
3. Obtain hardcopy printout of test results.
4. Use the Model 532 in the stand-alone mode.

In the production test of complex, microprocessor-based products, it is desirable to monitor as many critical signals as possible and to provide a high degree of automation in order to enhance production test throughput.

9.3.1 PRODUCTION TEST OF A VIDEO GAME

Assume that the product to be tested is a new microprocessor-based video game. The low selling price of the product requires that all phases of production operate as efficiently as possible. In the production test area, it is mandatory that a simple GO/NO-GO test be used which can be monitored by low-skill-level personnel. In order to simplify system interconnection, maintenance ports designed to accept the Model 50 (or 51) probes have been incorporated into the product. (See Section 7.0.) In addition, capital equipment such as oscilloscopes and CRT's are not available.

For this application, the following test setup is suggested:

MODEL 532	SYSTEM-UNDER-TEST
A DATA CHANNEL	Microprocessor address bus (16 bits)
B DATA CHANNEL	I/O signals for character generators and joysticks

With this test setup, the Model 532 would first be operated with a known good production system and one or more auxiliary memory boards would be used to store a series of expected test results in UV PROMS (up to seven tests per board). Alternatively, the serial or parallel interface options can be used to download each test into the Auxiliary Memory Board's RAM, as required, from an off-line computer or controller.

In operation, the analyzer would be used in the stand-alone mode and would be set up to display signatures for GO/NO-GO testing. The product would then be exercised in its normal operating modes and appropriate tests would be recalled out of the auxiliary memory. New data would be collected, signatures computed, and any differences between the actual and expected signatures would flash on the screen. Thus, a steady signature is a GO indication; while a flashing signature represents a product failure. If required, the serial interface can be used to provide a hardcopy of the test results.

9.3.2 PRODUCTION TEST OF A PRINTER

Assume that the product to be tested is a new, microprocessor-based printer. The complexity of this type of product requires that the analyzer provide both a first-level GO/NO-GO test plus second-level isolation of faults. In order to simplify interconnection, maintenance ports designed to accept the Model 50 (or 51) probes have been incorporated into the product. In addition, IC test clips have been added to the Model 52 terminators to accommodate the testing of certain critical components.

For this application, the following test setup is suggested:

MODEL 532	SYSTEM-UNDER-TEST
A DATA CHANNEL	Microprocessor address bus (16 bits)
B DATA CHANNEL	Microprocessor data bus, status signals, and sensor and driver interfaces

With this test setup, the Model 532 would first be operated with a known good production system to capture expected test results into the auxiliary memory. Alternatively, external tests can be downloaded into the RAM on the Auxiliary Memory Board using the Serial (RS-232C/TTY) or Parallel (IEEE-488) Interface Board. In addition, a scope or CRT terminal would be useful to support subsequent fault diagnosis.

In operation, the first-level tests are of the GO/NO-GO variety using signature comparisons as described in Section 9.3.1. Then, when a fault is detected, additional tests can be recalled out of the auxiliary memory for more detailed analysis. For example, an intermittent print column can

easily be analyzed by triggering on the associated print subroutine while monitoring and comparing the signals to the print head drivers.

10.0 SPECIAL APPLICATIONS

Certain features of the Model 532, such as dual-clocking and user programmability, permit the instrument to be used in support of a variety of specialized tasks.

10.1 DUAL-CLOCKING

The Model 532 utilizes separate clocks for its A and B data input channels so that it can be used to analyze multiplexed busses. Such busses are becoming more common, particularly for the new generation of microprocessor chips (such as the 8085, 8086, Z-8000, etc.).

There are two fundamental conditions which must be satisfied when using the dual-clocking feature:

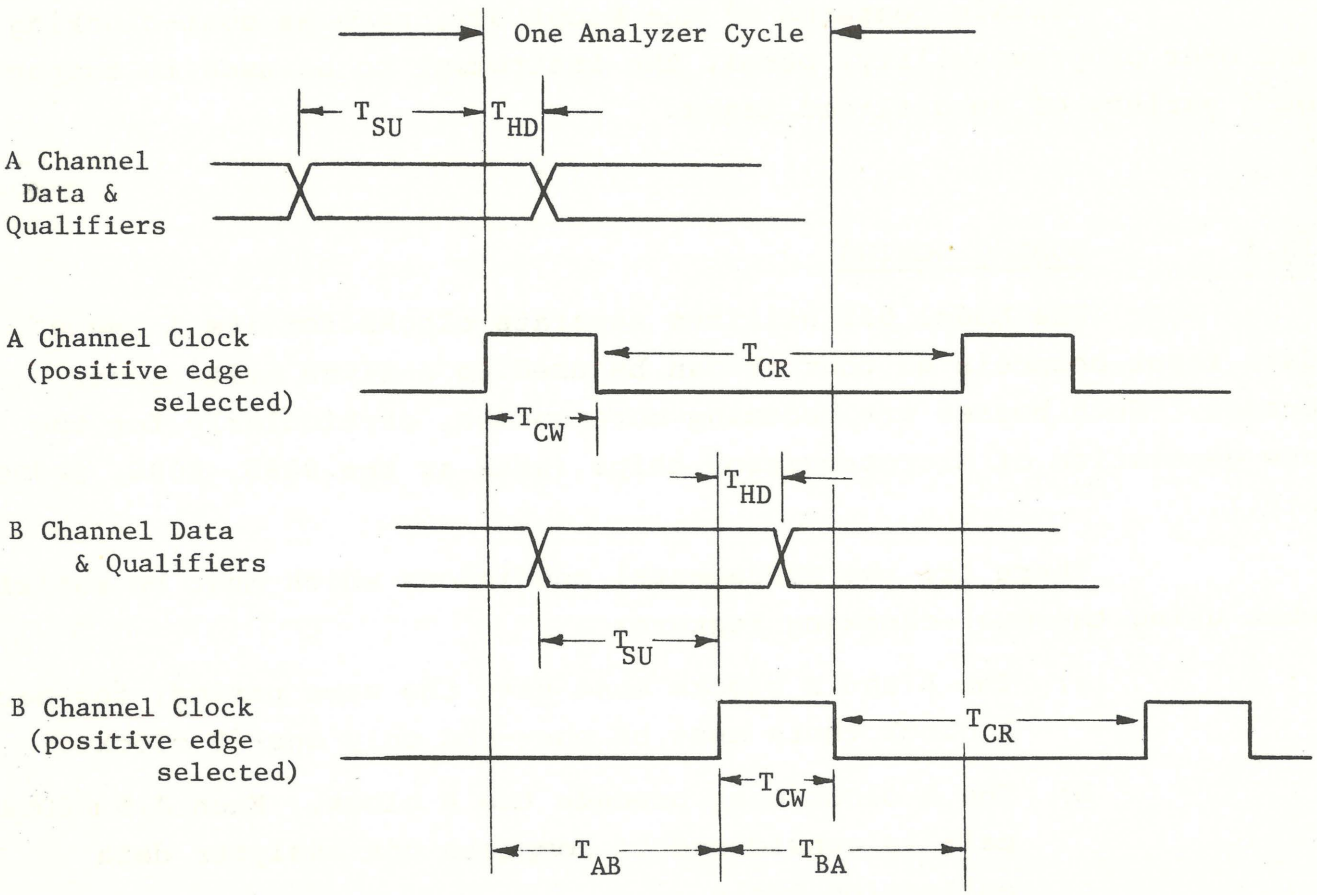
a) The A and B clocks must have the same period: for each A clock there must be one--and only one--B clock.

b) The A clock must precede the B clock. Each A,B CLOCK pair is considered to complete one analyzer data collection cycle.

Also, analyzer timing is referenced to the B clock. Fig. 10.1-1 illustrates the timing relationships which must be observed.

If the A and B timing relationships defined above are not observed, the placement of the A and B data words in the analyzer's memory will not be consistent. However, there may be some instances where this mode of operation can still be used--but the interpretation of the resulting display would require detailed knowledge of the phasing of the two input clocks.

In summary, dual clocking permits one word to be written into the A or B data memory for each qualified A or B clock pulse, respectively; and all trigger and analyzer state decisions are referenced to the B clock whose occurrence completes an individual data collection cycle.



SYMBOL	DESCRIPTION	VALUE
T_{SU}	Data Set-up -- time data must be stable prior to clock edge.	30ns
T_{HD}	Data Hold -- time data must remain stable after clock edge.	0ns
T_{CW}	Minimum clock pulse width.	20ns
T_{CR}	Clock recovery (minimum)	30ns
T_{AB}	Minimum A to B edge delay.	30ns
T_{BA}	Minimum B to A edge delay	30ns

Fig. 10.1-1. Dual Clocking Timing Requirements.

10.1.1 DUAL CLOCKING EXAMPLE - DEMULTIPLEXING THE 8085 µP

The 8085 is typical of third-generation microprocessor chips in that address and data multiplexing is utilized to conserve pins. The 8085, in particular, time-shares the lower address byte and the data byte using the same 8 pins. Since address and data information cannot be present simultaneously, a single clock will not suffice to capture complete microprocessor transactions directly from the chip: independent address and data clocks are required.

Although the following example specifically treats the 8085, it can easily be extended to other 8 or 16-bit microprocessor chips which multiplex address and data. In all cases, the Model 50 or 51 probes can be interfaced directly to the chip-under-test or to suitable address and data buffers in the system. For direct interfacing, a 40-pin DIP clip is recommended.

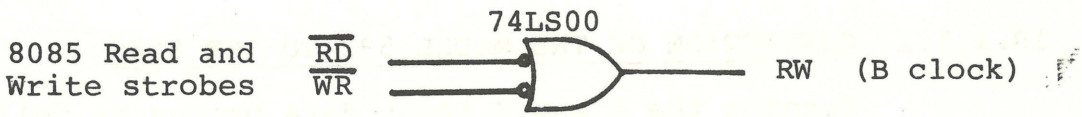
10.1.1.1 CONNECTION OF THE MODEL 532 TO THE 8085

Connect the A and B input data probes as follows:

A PROBE (Polarity set to TRUE)	8085 PINOUT
GND	Vss (µP GND)
D0-D7	AD0-AD7
D8-D15	A8-A15
Q_{TRIG}	S0
Q_{CLK}	NO CONNECTION
CLK	ALE

B PROBE (Polarity set to TRUE)	8085 PINOUT
GND	Vss (µP GND)
D0-07	AD0-A07
D8	S0
D9	S1
D10	I0
D11-D15	USER-DEFINED: AVAILABLE FOR ADD'L STATUS BITS
Q_{TRIG}	NO CONNECTION
Q_{CLK}	NO CONNECTION
CLK	RW* (SEE BELOW)

*A clock signal which assures one clock cycle for each ALE signal is required for dual clocking. This signal is easily synthesized with a simple 2-input NAND gate as follows:



10.1.1.2 MODEL 532 SETUP

Set the controls of the Model 532 as follows:

A TRIGGER WORD - Desired 16-bits µP address
A CLOCK - falling edge (↓)
A CLK QUALIFIER - X (don't care)
A TRIG QUALIFIER - as required (1 = READ, 0 = WRITE, X = don't care)
B TRIGGER WORD - Desired 8-bit data plus status as required.
B CLOCK - falling edge (↓)
B CLK QUALIFIER - X (don't care)
B TRIG QUALIFIER - X (don't care)

This setup will allow simultaneous monitoring of all 16 address bits, 8 data bits, plus I/O and status bits as required. The Model 532 will demultiplex address and data and display the information side-by-side.

10.2 INCREASING THE UPPER FREQUENCY OF THE MODEL 532

The dual clocking feature of the Model 532 permits the instrument to be used at twice its normal maximum clock frequency when limiting analysis to 16 channels of data. Thus, the Model 532A can be used at 10 MHz while the Model 532B can be used at 24 MHz.

The following describes the necessary setup:

1. Connect both A and B data input probes to the 16 lines to be monitored.
2. Connect both A and B clock inputs to the same clock which should be running at 1/2 the desired collection rate. For example, if one data sample is to be collected every 50 ns, the clock should have a period of 100 ns, or a frequency of 10 MHz. Note that the recommended minimum clock pulsewidth is 40 ns.
3. Set the A clock for a rising (⤴) edge and the B clock for a falling (⤵) edge.

All sequential-type triggering modes can be used at this higher frequency of operation since an "A before B" input is utilized. If the user is uncertain about the correct sequence of events relative to the clock, it may be required to reverse the rising and falling edge selection.

The resulting display will show all odd-numbered words in the A section and all even-numbered words in the B section.

10.3 USE OF THE CNTRL SIGNAL ON THE MODEL 50 AND 51 PROBES

Using special software, the CNTRL signal provides an active, user-defined output function in conjunction with otherwise passive probes. (It is also used with the dedicated microprocessor probes described in Section 11.0.)

The purpose of the CNTRL signal is to provide control and

monitoring functions for the system-under-test. This signal is available at the Model 50 and 51 edge connector, but not at the flying leads associated with the Model 52 probe terminator.

The A data channel CNTRL signal has an active TTL output with 24 mA sink capability. This signal can be activated by user software in the Model 532 to provide special commands to the system-under-test such as "CONFIGURE FOR SPECIAL TEST SUBROUTINE."

The B data channel CNTRL is a low-power Schottky TTL type of input signal. User software can monitor this input to sense special system configurations or responses.

Note that simultaneous use of both A and B CNTRL signals permits bidirectional "handshaking" transactions between the analyzer and the system-under-test. Consult the factory for additional information if you desire to use the Model 532 as both an input (passive) and output (active) analysis device.

10.4 SPECIAL MONITORING FUNCTIONS

Using dedicated probes and accessories, the Model 532 has been designed to support a variety of special monitoring functions.

10.4.1 SERIAL INTERFACE MONITORING

In applications where it is necessary to monitor the transactions occurring at a serial interface--such as an RS-232C port--a special serial-to-parallel converter probe can be used. Thus, serial information, such as ASCII characters, will then be captured and listed in sequence in the resulting display.

10.4.2 ASYNCHRONOUS PARALLEL INTERFACE MONITORING

For asynchronous, parallel I/O data transfers--such as

those associated with the IEEE-488 bus--the Model 532 will interface with a special I/O probe which performs the required buffering and synchronization functions.

10.4.3 GLITCH CAPTURE ACCESSORY

The Model 60 Glitch Capture Accessory is an option which permits detecting state changes which are asynchronous with the system clock. The Model 60 interfaces between the Model 532 and the standard Model 50 or Model 51 probes. When it is switched off, the Model 60 has no effect on analyzer operation. When it is activated, any glitch of 10 ns (or greater) duration will be displayed as a state change on the next successive clock cycle. This glitch capture mode can be used to:

1. Provide detection of transient and illegal state transitions. For example, it can be used to detect the "metastable" condition of a synchronizer.
2. Trigger the analyzer and collect data on a state change which occurs at a higher clock rate than the normal sampling clock.

10.5 EXPANSION OF THE MODEL 532 BEYOND 32 BITS

The Model 532 incorporates an expansion connector at the rear panel which contains three open collector trigger signals: one for the A data channel, another for the B sequential comparator, and a third for the B parallel comparators. Also brought out is the open collector RESET bus for synchronizing the two analyzers.

With these signals, two Model 532's can be ganged together by simply connecting the expansion port of both units together with a 10-conductor flat ribbon jumper (available as an option). User jumpers should be kept less than 6" (15 cm) in length to avoid capacitive loading of the comparator signals. When two units are ganged in this

manner, they should be connected to the system-under-test as follows:

A data channel inputs of both analyzers: Monitor A data (32 bits)

A data channel clocks: Both A clock inputs and A clock qualifiers are connected to the same point. A clock polarity setting for each analyzer must be the same.

B data channel inputs of both analyers: Monitor B data (32 bits)

B data channel clocks: Both B clock inputs and B clock qualifiers are connected to the same point. This is not necessary if the A clock is selected for both B data channels. However, B clock settings must be identical.

Designate one analyzer as the master and the other as the slave. The slave must have the DISPLAY TIME/HOLD control set to the HOLD position.

Always set both analyzers for the same triggering mode and the same delay. Note that for ganged operation, the trigger word is now 64 bits long. Therefore, for the parallel triggering mode, a 64-bit parallel word plus 4 trigger qualifiers can be used to specify the trigger. For the sequential mode, two sequential 32-bit words plus 2 sets of trigger qualifiers specify the triggering mechanism.

The RESET bus and associated synchronization circuitry assure that both analyzers are synchronized regardless of minor timing differences between the two units.

For display purposes, any combination of stand-alone and CRT presentations can be used.

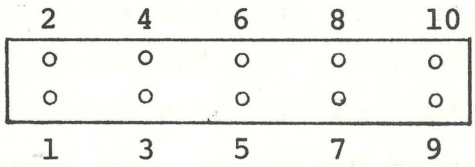
10.6 REMOTE CONTROL OF DATA COLLECTION USING EXTERNAL RESET

There is a class of applications where it is desirable to control data collection upon the occurrence or nonoccurrence of a specific event. For example, the "watch-dog" timer present in some computers is usually initialized to a specific value at specified times by operating system software. The timer interval is set by software so that a time-out can never occur in normal computer operation. However, if a hardware or software fault occurs which causes the operating system software to miss the initializing event, the timer will time-out and indicate a failure on the front panel or monitoring equipment.

In this type of application, the data collection mode of the Model 532 can be externally controlled by the pulse which initializes the watch-dog timer. Thus, in the event of a software or hardware failure, the analyzer would contain the data collection which preceded the absense of the initialization pulse.

In order to implement this type of external control, the analyzer's RESET line, which is available at the expansion port, can be utilized. This line is an open-collector, TTL level internally pulled-up with a 1K resistor to +5V. A low-going logic level (with a minimum pulsewidth of 30ns) on this input will force the analyzer into the RESET state. This state is synchronized by the clock of the system-under-test and will remain stable until one clock cycle following the externally applied pulse. At this point, a new data collection will be initiated. When using this mode of operation, the DISPLAY TIME/HOLD control on the Model 532's front panel must be in the HOLD position.

The following diagram will aid in identifying the signals on the Model 532's expansion port, which is located at the rear of the unit. (See Fig. 4.3-1). Connection to this port is easily made using a compatible 10-conductor flat ribbon header (3M or equivalent), or by using individual pin connectors like the Berg pins used with the Model 52 probe terminator.



BOTTOM

(rear view)

EXPANSION PORT SIGNALS

Pin No.	Signal
1,3,5,7	GROUND
2	A DATA CHANNEL COMPARATOR (open-collector)
4	RESET BUS (open-collector)
6	B PARALLEL COMPARATOR (open-collector)
8	B SEQUENTIAL COMPARATOR (open-collector)
9,10	NO CONNECTION

Fig. 10.6-1. Model 532 expansion port signal definitions.

* * *

Consult the factory for the status and availability of the various options and accessories described in Section 10.0.

10.7 USER-DEFINED KEYS

Two spare keys, * and □, are used with the optional User's Program Memory Board. Without this board plugged in, these keys have no effect. With the board inserted, the * key causes the Model 532 main program to execute the instruction at E000, which is in the User's Program Memory Board's memory space. The instruction at E000 must be an unconditional jump to the user-defined subroutine.

The □ key operates the same way except the initial jump is to E004.

11.0 MICROPROCESSOR SYSTEM DEVELOPMENT APPLICATIONS

The Model 532 will support microprocessor system development applications through the use of special dedicated probes. These probes permit the following function to be performed.

1. READ, WRITE, BREAKPOINT, RUN, HALT, and SINGLE STEP.
2. Trace and display CPU registers; modify CPU registers, transfer data between the microprocessor's memory and a terminal; and list, modify, and transfer memory blocks.

Dedicated probes for major microprocessors such as the 8080, 8085, 6800, and others are under development. As these probes are developed, the specifications, user instructions, and applications will be provided. Consult the factory for status and availability of these items.

12.0 THE WARRANTY

LIMITED WARRANTY

This warranty becomes valid only after the WARRANTY REGISTRATION CARD, packed with each unit, is filled out and mailed to Paratronics, Inc. (hereinafter P.I.) within ten (10) days from the data of equipment delivery.

Your analyzer instrument is guaranteed against all defects in materials and workmanship for a period of one (1) year from the date of delivery to the original user. All instruments returned to P.I. POSTPAID during the one year period will be replaced or restored to proper working condition and returned to the sender without charge.

NOTE: THIS WARRANTY DOES NOT APPLY TO DAMAGE CAUSED BY SHIPPING, ACCIDENT, UNAUTHORIZED REPAIR, ABUSE, MISUSE, OR MODIFICATION; OR TO INCONVENIENCES OR CONSEQUENTIAL DAMAGES OCCASIONED BY THE INSTRUMENT, OR BY BREACH OF ANY EXPRESSED OR IMPLIED WARRANTY WITH RESPECT THERETO. FURTHER, NO AGREEMENT EXTENDING OR MODIFYING THIS WARRANTY IN ANY WAY WHATSOEVER WILL BE BINDING UPON P.I. UNLESS EXECUTED BY A DULY AUTHORIZED OFFICER OF THE COMPANY.

This warranty gives you specific legal rights, and you may also have other rights which depend on local jurisdiction.

NOTE

DO NOT RETURN ANY EQUIPMENT TO THE FACTORY WITHOUT PRIOR AUTHORIZATION. SEE SECTION 3.5.

APPENDIX

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APPENDIX 1

A.1 ABBREVIATED DEMO PROCEDURE

REFER TO SECTIONS 4 AND 5 OF THIS MANUAL FOR ADDITIONAL INFORMATION.

PART I - BASIC DEMO

SET-UP

1. Connect the A&B probes to the Model 532. Connect the A probe for self-test and set up the scope for an X-Y display. Set the probes to TRUE. (If the Model 51 probes are used, set them both to TTL.)
2. Make certain all switches are centered--except SWITCH 1 which should be set to (↓) and SWITCH 6 which should be set to MAIN. Set CONTROL 1 to point to the left (approx. 10:00).
3. Turn power on. Adjust the scope and/or the analyzer's gain and positioning controls for a "clean" truth table. The OVERRIDE LED should be on, indicating that the analyzer is under internal, automatic control. Verify that the A and B displays and the scope show the correct self-test signature. (See test tag or front of Model 532 Manual.)
4. Move SWITCH 9 to RESET to gain control of the front panel. Then press the TRIG key (above SET DLY key) to enter the TRIG mode. The A display should now show 0040 and the B display should be blank (don't care). This is the starting point of the self-test program. (Note that a new signature is now on the scope--this is the unique signature of the TRIG mode.)

DISPLAYING THE DATA IN THE ANALYZER'S MEMORY

1. Move SWITCH 5 UP or DOWN to display different 16-word "pages" of the data memory. Return to the first page (labeled "TRIG" on scope screen).
2. Move SWITCH 8 to A BIN and then to B BIN to display 1's and 0's. Return to HEX mode.

DEMONSTRATING THE PARALLEL (32-BIT) TRIGGER MODE: (A,B)

1. Set the TRUE/COMPLEMENT switch on the B probe as follows: Model 50-TRUE; Model 51-COMPLEMENT.
2. Press the SET B key followed by F-F-F-F.
3. Move SWITCH 11 to CLOCK and increment SWITCH 10 by three counts so that the DELAY COUNT is 0003. The A and B DISPLAYS should read the 32-bit trigger word 0040 and FFFF; while the truth table should start at 0042, FFFF; or 3 program steps from the trigger word.

4. Press the CTL key followed by the WORD key to demonstrate the STAND-ALONE (or line-by-line) display mode. Verify that the first word in the data memory is indeed 0042, FFFF. Then increment SWITCH 10 to display other words in the data memory. Return to WORD 0 by decrementing SWITCH 10 to 0000. Now press SIG to view the distinct signature of this new data collection. Finally, press the TRIG key to view the trigger word (0040, FFFF) in the A and B DISPLAYS and 0003 in the DELAY COUNT readout, as before.

5. Move the TRUE/COMPLEMENT switch on the B probe to the opposite position. Note that the truth table disappears and the ARMED LED turns on. The analyzer will not trigger since the trigger requirement (0040, FFFF) is not satisfied.

DEMONSTRATING THE PARALLEL (32-BIT) TRIGGERING MODE: (A,$\overline{B}$)

1. Press the (A,$\overline{B}$) key and note that the analyzer triggers with the B side of the truth table now containing all 0's instead of all F's. Thus, the analyzer is triggering on the nonoccurrence of B. The main point here is that this mode is extremely useful for triggering on a failure mode, even though the failure mode is not known in advance.

PART II - ADVANCED DEMO

DEMONSTRATING THE SEQUENTIAL (16-BIT) TRIGGERING MODE: (A=B)

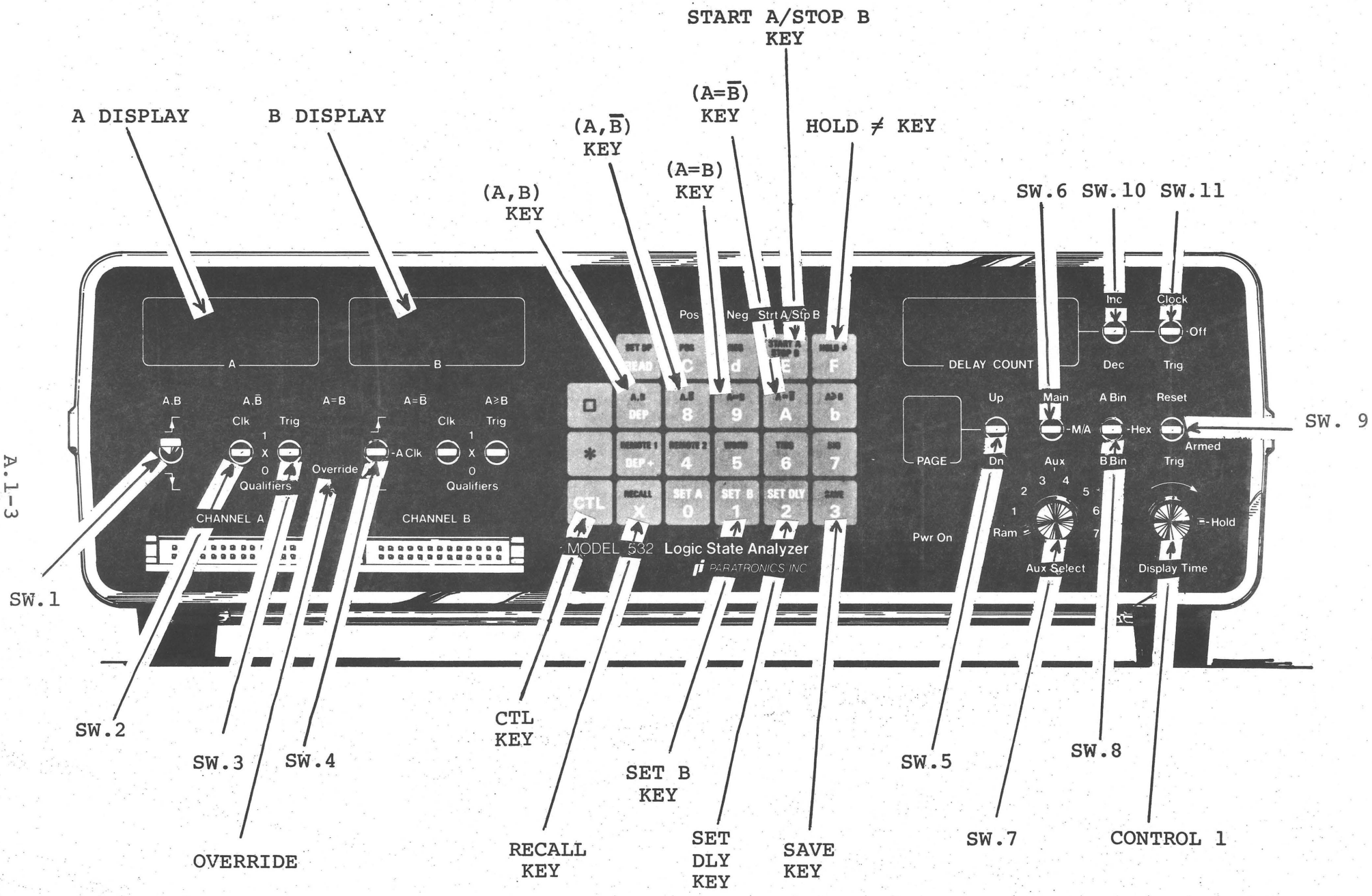
1. Press the (A=B) key (next to A,$\overline{B}$).
2. Press SET B followed by 0-0-4-3. Note that the ARMED LED comes on and the truth table goes blank. In this mode, the B trigger word is an event in the A channel which is separated from the A trigger word by a predetermined number of delay counts. Therefore, increment SWITCH 10 to 0004 and the analyzer will trigger. Note that this method can be used to find the number of program steps between two events in the A channel.

DEMONSTRATING THE SEQUENTIAL (16-BIT) TRIGGERING MODE: (A=$\overline{B}$)

1. Press CTL followed by (A=$\overline{B}$) and note that the analyzer does not trigger.
2. In this mode, the analyzer will not trigger as long as the correct B trigger word (0043) follows A (0040) by the correct number of delay counts (0004). If either the B value or the delay count value were to change, as would happen when an unknown failure occurred, the analyzer will trigger and display the failure. For example, increment the delay count value to 0005 by pressing SWITCH 10. Note that the analyzer now triggers.
3. Return to a DELAY COUNT value of 0000 by pressing the CTL key and then the SET DLY key followed by 0-0-0-0. (This demonstrates the use of the keyboard for setting in a delay value.)

DEMONSTRATING THE SEQUENTIAL (16-BIT) TRIGGERING MODE: START A/STOP B

1. Press the CTL key followed by SET B and 0-0-4-2. Then press the CTL key followed by the START A/STOP B key. Note that the truth table shows only 4 words in the data memory, since the analyzer starts collecting when A (0040) occurs and stops when B (0042) occurs. Also note that the display does not blink since only 4 words (instead of 250) are being processed for each data collection.


START A/STOP B KEY
A DISPLAY
B DISPLAY
(A=B̄) KEY
(A,B̄) KEY
HOLD ≠ KEY
(A,B) KEY
(A=B) KEY
SW.6 SW.10 SW.11
SW. 9
SW.1
SW.2
SW.3
SW.4
OVERRIDE
CTL KEY
RECALL KEY
SET B KEY
SET DLY KEY
SAVE KEY
SW.5
SW.7
SW.8
CONTROL 1
A
B
A,B
A,B̄
A=B
A=B̄
A≥B
Clk
Trig
Qualifiers
Override
-A Clk
CHANNEL A
CHANNEL B
Pos
Neg
Strt A/Stp B
DELAY COUNT
Inc
Clock
Off
Dec
Trig
PAGE
Up
Dn
Main
A Bin
Reset
-M/A
-Hex
Armed
Aux
B Bin
Trig
Ram
Aux Select
Display Time
Hold
Pwr On
MODEL 532 Logic State Analyzer
PARATRONICS INC

2. Press the WORD key and increment SWITCH 10 to view the same data in the A and B displays, one line at a time. Press the SIG key to view the associated signatures. The START A/STOP B mode is useful for capturing a limited sequence such as a subroutine whose starting point is ADDRESS A and whose STOPPING point is ADDRESS B. Return to the TRIG mode by pressing the TRIG key.

DEMONSTRATING THE AUXILIARY MEMORY

1. Move SWITCH 2 between the 0 and X position and note that the 3rd line of the truth table can be deleted. This line represents an 8085 I/O address which is used to identify the Model 532's current software revision number. The A clock qualifier line, which is controlled by SWITCH 2, is connected for self test so that a logic 1 level accompanies each I/O address. Therefore, switching the A clock qualifier (SWITCH 2) to 0 will delete I/O operations from the program flow.
2. With SWITCH 2 set to X, move SWITCH 7 to the RAM position and press the SAVE key to store the 4 words in the RAM. (Of course, up to 250 words can be stored in the RAM and each PROM memory element.)
3. Move SWITCH 6 to AUX to view the data in the RAM. Then move SWITCH 6 to M/A to verify that the data in the main and RAM memories are the same. Leave SWITCH 6 in the M/A position.
4. Now move SWITCH 2 to 0 to again delete the 3rd line. Note the flashing data and signatures. Also move SWITCH 8 to A BIN and back to HEX.
5. Press CTL and SET A followed by 1-2-3-4 to enter a nonvalid trigger word. This will cause the truth table to disappear and the ARM LED to turn on Also press CTL and the (A,B) key to change modes.
6. Press RECALL to duplicate the particular test stored in Step 2. Note that the A and B displays automatically show 0040 and 0042, as before, and that the mode changes back to START A/STOP B. Note also that the OVERRIDE LED is on, indicating that the front panel controls affecting the entry of trigger modes are inhibited. In order to demonstrate this, repeat Step 5 and observe that there is no affect.
7. Press RESET to gain control of the front panel and note that the OVERRIDE LED turns off.
8. With SWITCH 2 at X, press CTL and the HOLD ≠ key. Now move SWITCH 2 between X and 0 and note that the truth table now continues to flash even when SWITCH 2 is back in the X position. Thus, in the HOLD ≠ mode, the analyzer continually holds and compares the first real-time data collection which differed from the data stored in the RAM. This mode is extremely powerful for catching intermittent problems.

APPENDIX 2

A.2 HEXADECIMAL CONVERSION AIDS

F E D C		B A 9 8		7 6 5 4		3 2 1 0	
Hex	Decimal	Hex	Decimal	Hex	Decimal	Hex	Decimal
0	0	0	0	0	0	0	0
1	4,096	1	256	1	16	1	1
2	8,192	2	512	2	32	2	2
3	12,288	3	768	3	48	3	3
4	16,384	4	1,024	4	64	4	4
5	20,480	5	1,280	5	80	5	5
6	24,576	6	1,536	6	96	6	6
7	28,672	7	1,792	7	112	7	7
8	32,768	8	2,048	8	128	8	8
9	36,864	9	2,304	9	144	9	9
A	40,960	A	2,560	A	160	A	10
B	45,056	B	2,816	B	176	B	11
C	49,152	C	3,072	C	192	C	12
D	53,248	D	3,328	D	208	D	13
E	57,344	E	3,584	E	224	E	14
F	61,440	F	3,840	F	240	F	15

HEX ARITHMETIC TABLES

ADDITION TABLE

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
2	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11
3	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12
4	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
5	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14
6	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15
7	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16
8	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17
9	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18
A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19
B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A
C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B
D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C
E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D
F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E

MULTIPLICATION TABLE

1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
2	04	06	08	0A	0C	0E	10	12	14	16	18	1A	1C	1E
3	06	09	0C	0F	12	15	18	1B	1E	21	24	27	2A	2D
4	08	0C	10	14	18	1C	20	24	28	2C	30	34	38	3C
5	0A	0F	14	19	1E	23	28	2D	32	37	3C	41	46	4B
6	0C	12	18	1E	24	2A	30	36	3C	42	48	4E	54	5A
7	0E	15	1C	23	2A	31	38	3F	46	4D	54	5B	62	69
8	10	18	20	28	30	38	40	48	50	58	60	68	70	78
9	12	1B	24	2D	36	3F	48	51	5A	63	6C	75	7E	87
A	14	1E	28	32	3C	46	50	5A	64	6E	78	82	8C	96
B	16	21	2C	37	42	4D	58	63	6E	79	84	8F	9A	A5
C	18	24	30	3C	48	54	60	6C	78	84	90	9C	A8	B4
D	1A	27	34	41	4E	5B	68	75	82	8F	9C	A9	B6	C3
E	1C	2A	38	46	54	62	70	7E	8C	9A	A8	B6	C4	D2
F	1E	2D	3C	4B	5A	69	78	87	96	A5	B4	C3	D2	E1

A.2.3 OCTAL TO HEX CONVERSION CHART

OCTAL	BINARY
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

HEX	BINARY
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
A	1010
B	1011
C	1100
D	1101
E	1110
F	1111

Example: Convert (7412) OCT to HEX equivalent

Procedure:

7	4	1	2	OCTAL WORD
111	100	001	010	OCTAL BINARY GROUPING

(Extra Zeroes → 0000)	1111	0000	1010	HEX BINARY GROUPING
0	F	0	A	HEX WORD

Thus: (7412) OCT = (0F0A) HEX

APPENDIX 3

A.3 RS-232C/TTY SERIAL INTERFACE BOARD (SIB) OPTION

The Model 532 RS-232C/TTY Serial Interface Board (SIB) option permits remote analyzer programming, display, and/or printout. This option is intended for use where an oscilloscope-type display is not available or desirable, or where remote control functions are required--such as in field service applications. It is also useful in production test where hardcopy output may be an essential part of a product acceptance test program. The SIB may also be used in an R&D environment where a video terminal is the focal point in a microprocessor development system.

The SIB option may also be ordered, or user-configured, to provide a 20 mA current loop TTY interface.

A.3.1 SIB CONFIGURATION

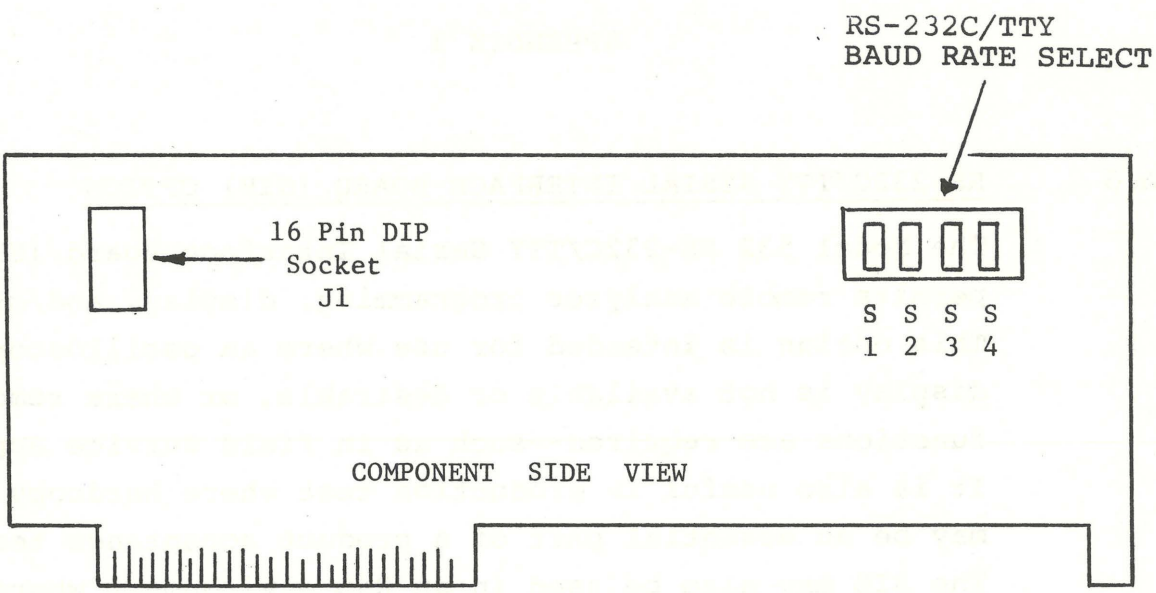
The SIB may be user-installed without any electrical modifications to the analyzer itself. However, before installation, the board must be configured for RS-232C or TTY operation as described below.

A.3.1.1 RS-232C OPERATION

The SIB is configured for RS-232C operation at the factory unless the TTY configuration is specified by the user. For correct RS-232C operation, the baud rate select switch on the SIB must be set to a value compatible with the peripheral device used. The baud rate range is 50 baud to 9.6K baud. Fig. A.3.1.1-1 illustrates the location of the switch.

NOTE

REFER TO SECTION A.3.2 FOR SERIAL INTERFACE BOARD INSTALLATION INSTRUCTIONS.



BAUD RATE	S1	S2	S3	S4
110	U	U	U	U
150	D	U	U	U
300	U	D	U	U
2400	D	D	U	U
1200	U	U	D	U
1800	D	U	D	U
4800	U	D	D	U
9600	D	D	D	U
2400	U	U	U	D
600	D	U	U	D
200	U	D	U	D
134.5	D	D	U	D
75	U	U	D	D
50	D	U	D	D

U = Switch lever up toward top of case

D = Switch lever down toward mother board

Fig. A.3.1.1-1. RS-232C/TTY baud rate select switch and DIP socket locations.

A.3.1.2 TTY OPERATION

If the SIB is configured for RS-232C operation, the following modifications are required for the 20 mA current loop interface:

1. Install jumpers J7 and J8.
2. Install resistor R12 (470-ohm, 1/4W, 5%).
3. Modify the RS-232C connector as follows:
   a. Connect the TTY magnet between pins 4(+) and 3(-).
   b. Connect the TTY keyboard (normally closed) between pins 2 and 14.
   c. Connect a jumper wire between pins 20 and 6.

For this mode, the TTY itself must be configured for common full duplex (4-wire) operation, and the baud rate select switch must be properly set as described in Section A.3.1.1 above.

WARNING

WHEN THE SIB IS SET FOR TTY OPERATION, DO NOT PLUG RS-232 EQUIPMENT INTO THE SERIAL INTERFACE CONNECTOR OF THE MODEL 532.

A.3.1.3 SERIAL PROTOCOL

The USART initialization software in the SIB configures the USART for a specific protocol as described below. The terminal that is interfaced to the 532 should be set up using a compatible protocol.

SIB Standard Protocol:

Mode: Asynchronous, full duplex
Parity: No parity
Character Length: 8 bits
Stop Bit Length: 2 bits
Baud Rate: Selectable 50-9600 baud

Other protocols within the 8251 USART capabilities can be supplied on special order. Consult the factory.

A.3.2 SIB INSTALLATION

When field-installing the SIB option, the following steps should be followed:

1. With the power cord removed, loosen the two captive fasteners at the top of the Model 532 case and slide the top cover back.
2. Install the RS-232C connector assembly by placing the 16-pin DIP plug through the rear panel cutout. The connector itself mounts with the hardware provided on the outside of the rear panel. See Fig. A.3.2-1.
3. Inset the SIB into the third Model 532 bus slot--from the right as you face the unit--and insert the DIP plug in the mating socket near the top of the board. See Fig. A.3.1.1-1.

A.3.3 DESCRIPTION OF TERMINAL

The Model 532 serial interface option requires a full duplex terminal with a minimum carriage width of 40 columns and a standard ASCII character set. Note that receiving and transmitting speeds must be equal and are set with the baud rate switch on the SIB. See Section 3.1.3 for proper serial protocol.

A.3.4 INITIALIZATION

When the Model 532 is first turned on, it will be in the self-test (LOCAL) mode and no serial (or IEEE-488) control is possible. With the terminal connected to the Model 532 via the rear interface connector, the serial mode can be activated by pressing RESET followed by the CTL key and the REMOTE 1 key on the analyzer's keyboard. At that time, the following sequence of events will occur:

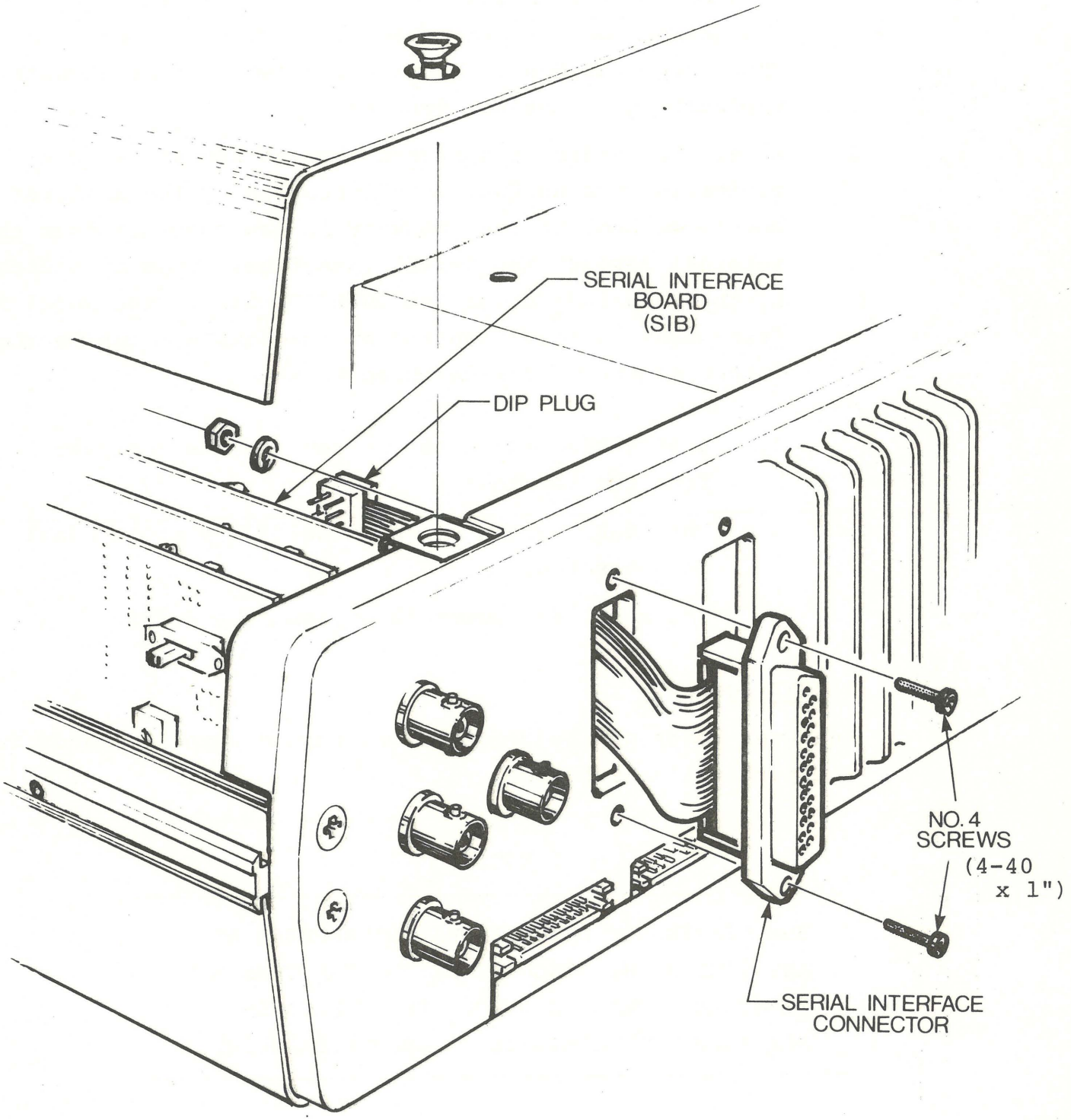


Fig. A.3.2-1. Installation of serial interface connector.

1. A header is transmitted to the terminal. (Note that this header can be customized for "sign-on" purposes when using the Model 532 with a modem in remote control applications. Consult factory.)

2. After the header, a software version number is sent indicating the software configuration of the analyzer. Remote control of the analyzer is now possible from the terminal through the serial interface. This is indicated by the illumination of the OVERRIDE LED on the Model 532's front panel. Local control of the analyzer can be regained in one of the following three ways:

    1. A RELEASE command (R) is sent to the analyzer from the terminal.
    2. The RESET switch on the Model 532's front panel is activated.
    3. The Model 532 power is cycled on and off.

A.3.5 REMOTE COMMANDS

Analyzer modes can be remotely programmed using commands from the terminal's keyboard.

NOTE

THE LISTING OF DATA CAN BE INTERRUPTED AT ANY TIME BY HITTING ANY KEY ON THE TERMINAL'S KEYBOARD. THIS IS USEFUL IF IT BECOMES NECESSARY TO TERMINATE A LENGTHY PRINTOUT.

ANALYZER COMMAND	REMOTE KEYBOARD ENTRY	DESCRIPTION
SET A TRIGGER	A nnnn cqt	nnnn = 4-digit hex value: O-F,X c = clock edge: P (rising) N (falling) q = clock qualifier: 1,0,X t = trigger qualifier: 1,0,X Example: A 0040 PXX (Set A to 0040, positive clock edge, qualifiers = don't care.)
SET B TRIGGER	B nnnn cqt	nnnn = 4-digit hex value: O-F,X c = clock edge: P (rising); N (falling); or A (use A clk for B data channel) q = clock qualifier: 1,0,X t = trigger qualifier: 1,0,X Example: B FFFF AXX (Set B to FFFF; use A clock; qualifiers = don't care.)
SET DELAY VALUE & MODE	D nnnn X	nnnn = 4-digit decimal value 0000-9999 X = C clock delay T trigger delay Example: D 0003 C (Set delay value to 0003; use CLOCK DELAY mode.)

NOTE

ONLY LAST 4 DIGITS ENTERED IN FOR nnnn ARE ACCEPTED FOR TRIGGER WORD OR DELAY. ALSO, DATA IS ALWAYS RIGHT JUSTIFIED, E.G., A 35 TYPED IN IS INTERPRETED AS 0035. ALSO, THE SPACE KEY MUST BE DEPRESSED TO DESIGNATE THE END OF ANY DATA ENTRY.

ANALYZER COMMAND	REMOTE KEYBOARD ENTRY	DESCRIPTION
SET TRIGGER MODE	M XXb t	XX = S START A/STOP B A, A,B A= A=B AG A≥ B b[1] = Blank (Trigger on occur- of B data word.) N (Trigger on nonoccur- of B data word. t = P POSITIVE TIME N NEGATIVE TIME
ARM ANALYZER FOR TRIGGERING	T	List Model 532 status and ARM. If triggering condition satisfied, the word "TRIGGERED" will appear.
LIST A & B DATA	L nnn mmm a	nnn = begin listing at this point in memory. mmm = end listing at this point. a = print AUX data also. (Leading 0's are assumed for integer values less than 3 digits long.) (Hit carriage return instead of "a" if you want to suppress aux. data.) Example: L 0 12 a (List MAIN and AUX memory between 000 and 012.)
LIST SIGNATURES	L S	The 4-digit hex signature pair associated with the analyzer's main and auxiliary memory will be displayed.
SELECT AUX MEMORY	U n	n = 0 RAM 1-7 PROM Example: U 0 (Use the RAM.)

[1]Type N only if the "nonoccurrence of B" modes are desired (e.g., A,$\overline{B}$; A=$\overline{B}$; etc.). Example: M A,N P (Set analyzer to A,$\overline{B}$ mode with post-trigger data collection.)

ANALYZER COMMAND	REMOTE KEYBOARD ENTRY	DESCRIPTION
SET HOLD ≠	H	Place analyzer in the HOLD ≠ mode and arm. Status of analyzer is printed out.
PROGRAM AUXILIARY	W	Program AUX MEMORY selected by U instruction. (AUXILIARY MEMORY BOARD programming voltage switch must be enabled to program selected PROM.)
RECALL AUXILIARY	C	Recall AUX MEMORY selected by U instruction.
RELEASE	R	Return analyzer to LOCAL control.
FORCE TRIGGER	F	Force analyzer to trigger.
LIST STATUS	S	Print all analyzer control settings and status on video terminal or printer.
LIST NOT EQUAL (LIST DIFFERENCES)	L D	Print only those words (and their displacements from the trigger word) which differ between main and selected aux. memory. A period at the end of a line is used to indicate a mismatch.

A.3.6 EXAMPLE

Connect the analyzer to a terminal and set in the correct baud rate. Configure the analyzer for self-test. (Leave the B data probe disconnected.) Turn power on, press the TRIG key and

and RESET the analyzer to gain full control of the front panel. Also, press the TRIG key to view the changes in analyzer triggering conditions when later requested from the terminal. Turn on the terminal and press the REMOTE 1 key on the analyzer to give control to the terminal. A header similar to the following should print out:

```
SERIAL INTERFACE ACTIVE VER. 1.1
M532 STATUS

MODE  A,B  POS
ATRIG 0040 P X X
BTRIG XXXX A X X
DELAY 0000 CLK
```

Next change the B trigger to FFFF as follows: (Don't forget to type A for A clock; and XX for setting the qualifiers to don't care--all triggering parameters must be retyped even though only one is being changed.)

```
?B FFFF A X X
BTRIG FFFF A X X
```

NOTE

THE "?" INDICATION IS GENERALLY USED TO TELL THE USER THAT THE ANALYZER HAS COMPLETED A TASK AND IS WAITING FOR FURTHER INSTRUCTIONS.

Next change the delay value to 3 clock delays by typing in D 3 C:

```
?D 3 C

DELAY 0003 CLK
```

Trigger analyzer and note that analyzer status is automatically printed out:

```
?T
M532 STATUS

MODE  A,B  POS
ATRIG 0040 P X X
BTRIG FFFF A X X
DELAY 0003 CLK
ARMED

?
TRIGGERED
```

List the first 6 words collected and note that the analyzer triggered at 0042, or 3 clock delays from 0040. (Remember to press RETURN after typing L 0 5.)

```
?L Ø 5
0000  0042 FFFF .
0001  0043 FFFF .
0002  0044 FFFF .
0003  0045 FFFF .
0004  100D FFFF .
0005  0046 FFFF .
```

Change the analyzer's triggering mode from (A,B; POS) to A=B; POS). Note that after M A= is typed by user, analyzer automatically provides B:

```
?M A=B P
MODE  A=B  POS
```

Set B to 0043 A XX:

```
?B Ø043 A X X
BTRIG Ø043 A X X
```

Now attempt to trigger analyzer by pressing T. Note that the analyzer does not trigger since the delay value must be 0004 to satisfy these particular trigger conditions:

```
?T
M532 STATUS

MODE  A=B  POS
ATRIG Ø040 P X X
BTRIG Ø043 A X X
DELAY Ø003 CLK
ARMED
```

Change delay value to 4 clock delays. Then press T again and note that the analyzer is now triggered:

```
?D 4 C

DELAY Ø004 CLK
?T
M532 STATUS

MODE  A=B  POS
ATRIG Ø040 P X X
BTRIG Ø043 A X X
DELAY Ø004 CLK

ARMED
?
TRIGGERED
```

List the first 3 words:

```
?L Ø 2
ØØØØ  ØØ43 FFFF .
ØØØ1  ØØ44 FFFF .
ØØØ2  ØØ45 FFFF .
```

Change the trigger mode to (A=$\overline{B}$; POS) and change the delay value back to 003. Then trigger the analyzer by pressing T. Note that this time the analyzer will trigger since 0043 is <u>not</u> 3 clock delays from 0040:

```
?M A=BN P
MODE  A=BN POS
?D ØØ3 C
DELAY ØØØ3 CLK
?T
M532 STATUS

MODE  A=BN POS
ATRIG ØØ4Ø P X X
BTRIG ØØ43 A X X
DELAY ØØØ3 CLK

ARMED
?
TRIGGERED
```

Change B to 0042 (note that the leading 0's can be left out):

```
?B 42 A X X
BTRIG ØØ42 A X X
```

Change the triggering mode to START A/STOP B. (After typing M S, the analyzer will automatically supply the remaining "ASB" characters.):

```
?M SASB
MODE SASB  POS
```

Now trigger the analyzer:

```
?T
M532 STATUS

MODE SASB  POS
ATRIG ØØ4Ø P X X
BTRIG ØØ42 A X X
DELAY ØØØ3 CLK

ARMED
?
TRIGGERED
```

Try to list all values between 0 and 10 and note that only the values between 000 and 003 are printed out since that is all the data presently in memory:

```
?L Ø 1Ø
0000  0040 FFFF •
0001  0041 FFFF •
0002  F1F1 FFFF •
0003  0042 FFFF •
```

List signatures. Note that 2 signature pairs are printed out and that the second pair corresponds to "garbage" data in the Aux. Memory:

```
?L S
SIG.  FBBE 0706  A477 7CFE
```

Use the RAM position of the Aux. Memory for storage by typing U 0:

```
?U Ø
```

Write the contents of the main memory into the RAM by typing W:

```
?W  AUX Ø
```

Now list main and aux. memory signatures again to see if the transfer was successful:

```
?L S
SIG   FBBE 0706  FBBE 0706
```

Next list the contents of the main and aux. memories between 0 and 4. Note that typing A at the end of the list request (instead of RETURN) causes the aux. memory contents to be included. Note also that WORD 4 was not collected and therefore is not included in the list:

```
?L Ø 4 A
0000  0040 FFFF  0040 FFFF
0001  0041 FFFF  0041 FFFF
0002  F1F1 FFFF  F1F1 FFFF
0003  0042 FFFF  0042 FFFF
```

Set the A clock qualifier to 0 to "qualify out" the I/O data line (WORD 002 in the previous data collection.):

```
?A 0040 P 0 X
ATRIG 0040 P 0 X
```

Perform a new data collection:

```
?T
M532 STATUS

MODE SASB  POS
ATRIG 0040 P 0 X
BTRIG 0042 A X X
DELAY 0003 CLK

ARMED

?
TRIGGERED
```

Now list the data between 0 and 003 in the main and aux memories. Note that a (.) indication appears at WORD 2 since this word was deleted from the main memory during the last collection and replaced by the next line (0042,FFFF):

```
?L 0 3 A
0000  0040 FFFF  0040 FFFF
0001  0041 FFFF  0041 FFFF
0002  0042 FFFF  F1F1 FFFF .
```

List only differences by press L D:

```
?L D
0002  0042 FFFF  F1F1 FFFF .
```

Press H to enter the (HOLD ≠) mode. Note that Model 532 status is automatically listed. Also, since the data being collected does not match the data in the RAM, a "HOLDING" indication is printed out. This tells the user an error exists between real-time and stored data which can be identified with the LIST or LIST DIFFERENCES modes described above:

```
?H
M532 STATUS

MODE SASB  POS
ATRIG 0040 P 0 X
BTRIG 0042 A X X
DELAY 0003 CLK

ARMED


?HØLDING
```

APPENDIX 4

A.4 IEEE-488 PARALLEL INTERFACE BOARD (PIB)

The PIB option is used to provide remote control of the Model 532 using the popular IEEE-488 bus. The control capabilities using this bus are similar to those realized by the serial interface described in Appendix 3.

The basic functions of the PIB are:

1. Remote operation of the Model 532 front panel.
2. Downloading of specific tests into the auxiliary memory RAM.
3. Remote or hardcopy listing of test results.

The PIB is configured by selecting TALKER and LISTENER addresses using DIP programming switches located on the board. Note that the PIB functions only as a "talker" or "listener," but not as a "controller."

Consult the factory for information concerning the availability of the PIB and the protocol of IEEE-488 bus operation.

APPENDIX 5

A.5 POWERS OF TWO TABLE

2^n	n	2^{-n}
1	0	1 0
2	1	0 5
4	2	0 25
8	3	0 125
16	4	0 062 5
32	5	0 031 25
64	6	0 015 625
128	7	0 007 812 5
256	8	0 003 906 25
512	9	0 001 953 125
1 024	10	0 000 976 562 5
2 048	11	0 000 488 281 25
4 096	12	0 000 244 140 625
8 192	13	0 000 122 070 312 5
16 384	14	0 000 061 035 156 25
32 768	15	0 000 030 517 578 125
65 536	16	0 000 015 258 789 062 5
131 072	17	0 000 007 629 394 531 25
262 144	18	0 000 003 814 697 265 625
524 288	19	0 000 001 907 348 632 812 5
1 048 576	20	0 000 000 953 674 316 406 25
2 097 152	21	0 000 000 476 837 158 203 125
4 194 304	22	0 000 000 238 418 579 101 562 5
8 388 608	23	0 000 000 119 209 289 550 781 25
16 777 216	24	0 000 000 059 604 644 775 390 625
33 554 432	25	0 000 000 029 802 322 387 695 312 5
67 108 864	26	0 000 000 014 901 161 193 847 656 25
134 217 728	27	0 000 000 007 450 580 596 923 828 125
268 435 456	28	0 000 000 003 725 290 298 461 914 062 5
536 870 912	29	0 000 000 001 862 645 149 230 957 031 25
1 073 741 824	30	0 000 000 000 931 322 574 615 478 515 625
2 147 483 648	31	0 000 000 000 465 661 287 307 739 257 812 5
4 294 967 296	32	0 000 000 000 232 830 643 653 869 628 906 25
8 589 934 592	33	0 000 000 000 116 415 321 826 934 814 453 125
17 179 869 184	34	0 000 000 000 058 207 660 913 467 407 226 562 5
34 359 738 368	35	0 000 000 000 029 103 830 456 733 703 613 281 25
68 719 476 736	36	0 000 000 000 014 551 915 228 366 851 806 640 625
137 438 953 472	37	0 000 000 000 007 275 957 614 183 425 903 320 312 5
274 877 906 944	38	0 000 000 000 003 637 978 807 091 712 951 660 156 25
549 755 813 888	39	0 000 000 000 001 818 989 403 545 856 475 830 078 125
1 099 511 627 776	40	0 000 000 000 000 909 494 701 772 928 237 915 039 062 5
2 199 023 255 552	41	0 000 000 000 000 454 747 350 886 464 118 957 519 531 25
4 398 046 511 104	42	0 000 000 000 000 227 373 675 443 232 059 478 759 765 625
8 796 093 022 208	43	0 000 000 000 000 113 686 837 721 616 029 739 379 882 812 5
17 592 186 044 416	44	0 000 000 000 000 056 843 418 860 808 014 869 689 941 406 25
35 184 372 088 832	45	0 000 000 000 000 028 421 709 430 404 007 434 844 970 703 125
70 368 744 177 664	46	0 000 000 000 000 014 210 854 715 202 003 717 422 485 351 562 5
140 737 488 355 328	47	0 000 000 000 000 007 105 427 357 601 001 858 711 242 675 781 25
281 474 976 710 656	48	0 000 000 000 000 003 552 713 678 800 500 929 355 621 337 890 625
562 949 953 421 312	49	0 000 000 000 000 001 776 356 839 400 250 464 677 810 668 945 312 5
1 125 899 906 842 624	50	0 000 000 000 000 000 888 178 419 700 125 232 338 905 334 472 656 25
2 251 799 813 685 248	51	0 000 000 000 000 000 444 089 209 850 062 616 169 452 667 236 328 125
4 503 599 627 370 496	52	0 000 000 000 000 000 222 044 604 925 031 308 084 726 333 618 164 062 5
9 007 199 254 740 992	53	0 000 000 000 000 000 111 022 302 462 515 654 042 363 166 809 082 031 25
18 014 398 509 481 984	54	0 000 000 000 000 000 055 511 151 231 257 827 021 181 583 404 541 015 625
36 028 797 018 963 968	55	0 000 000 000 000 000 027 755 575 615 628 913 510 590 791 702 270 507 812 5

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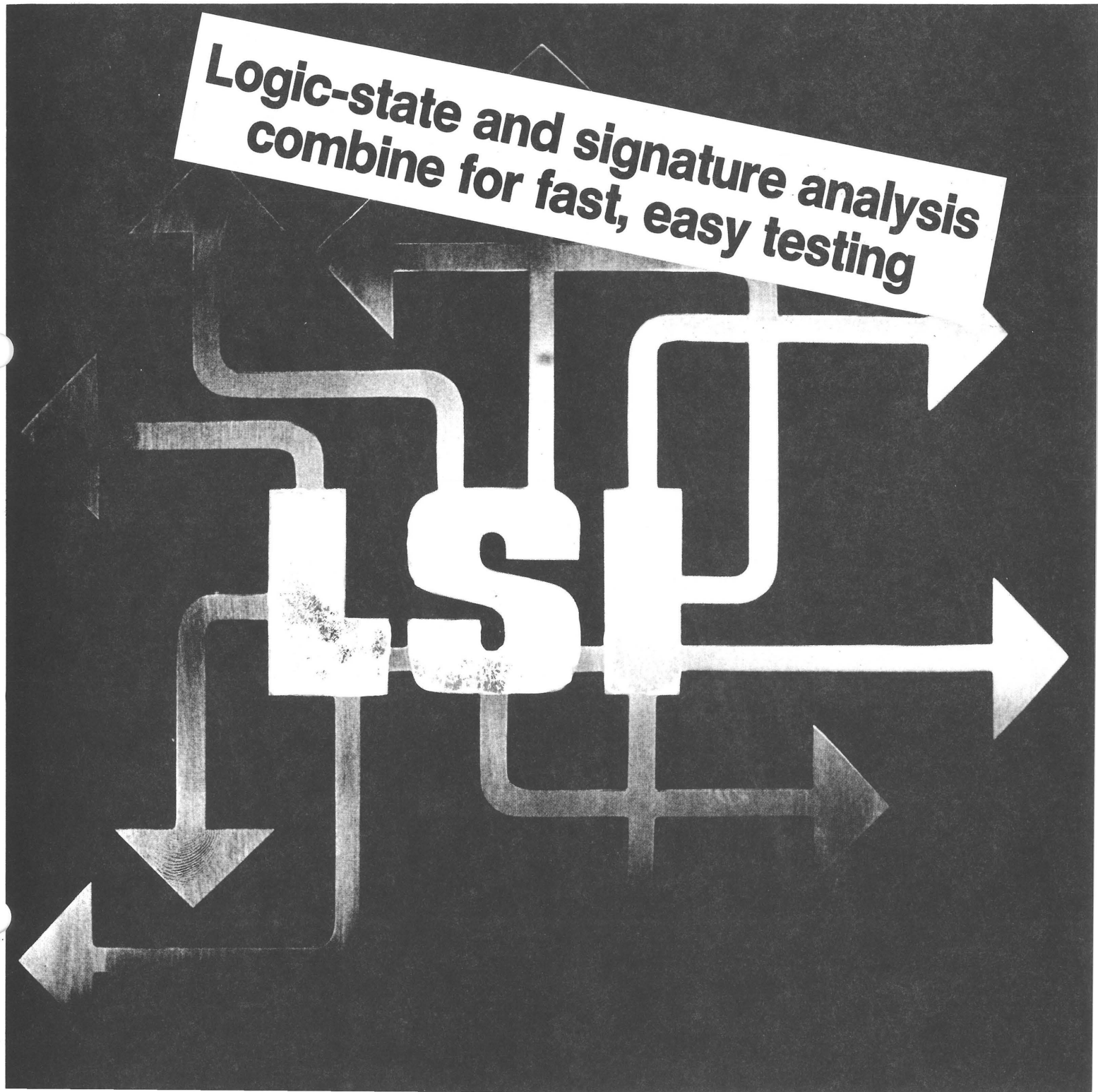

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ELECTRONICS, June 8, 1978

Logic-state and signature analysis combine for fast, easy testing

Microprocessor-based tester enhances logic-state analysis with signature-analysis algorithm that operates on stored data to find hardware and software faults quickly

by Ira H. Spector, *Paratronics Inc., San Jose, Calif.*

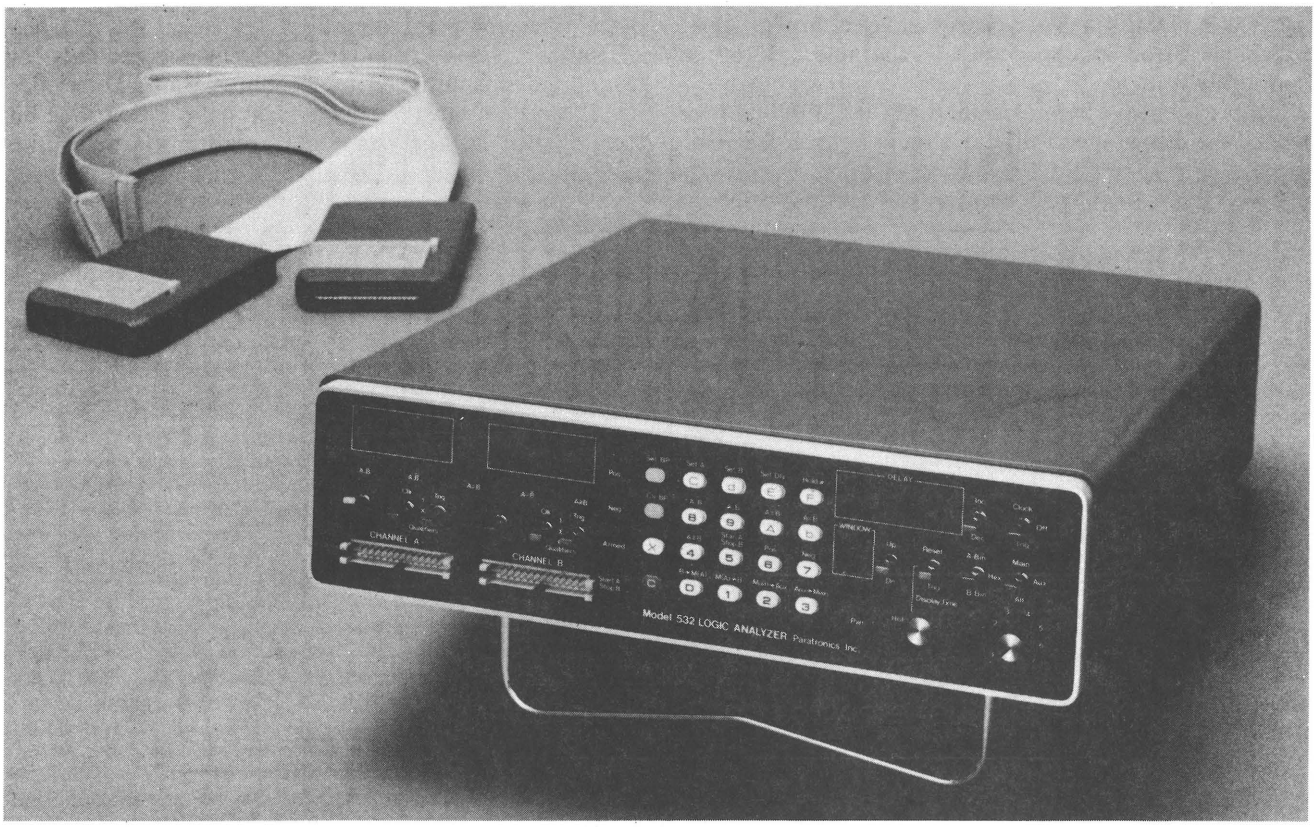
☐ Logic-state and signature analyzers have successfully defanged some nasty testing problems found in servicing microprocessor-based products. But they have done so separately. Thus the next step up in pacifying problems of field-service fault-finding for microcircuitry is a combination: logic-state analysis enhanced by a signature-analysis algorithm that operates on stored data to identify faults within a system under test. By combining the two, it is possible to analyze collected data more quickly and to eliminate the need for special test-support circuitry within the microprocessor-based product.

Logic-state analyzers (Fig. 1) are widely used to monitor sequential machine states and to help uncover many hardware problems such as soft address bits, missed flags, and intermittent control signals. In software debugging, the instruments have helped find programming errors, such as those responsible for sending the machine into some unwanted loop.

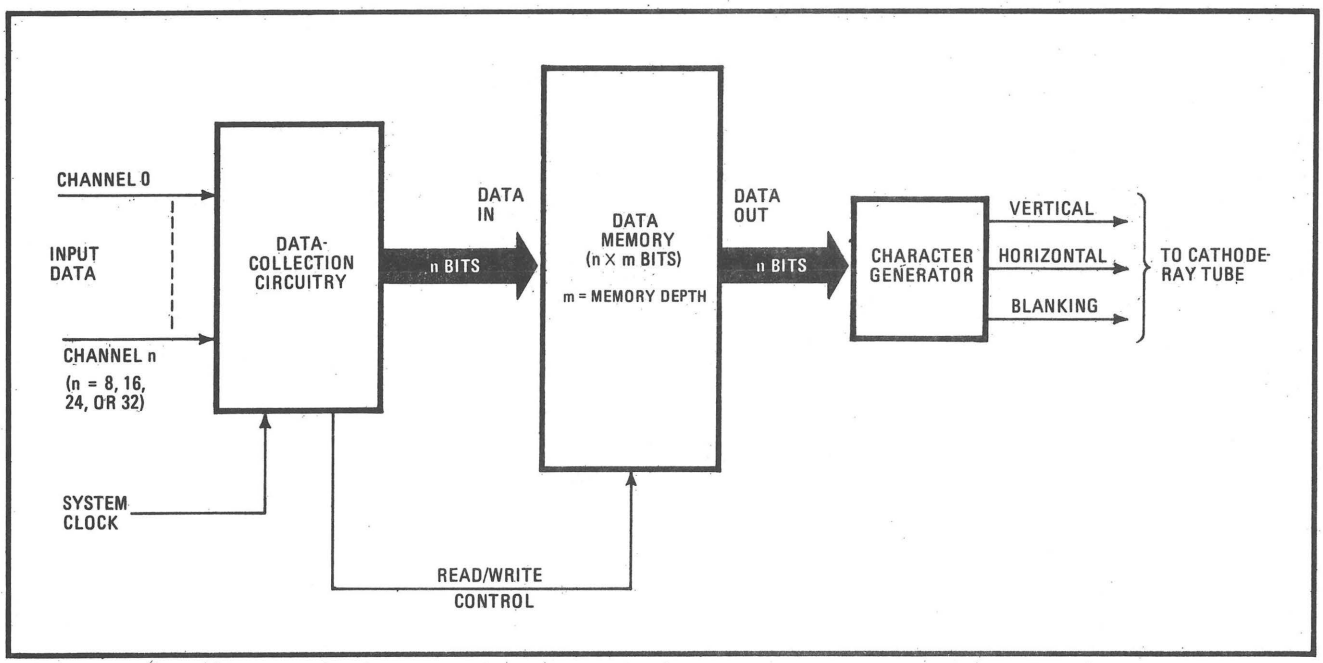
Spending time

However, these testers require the user to spend a great deal of time examining and analyzing captured data. The expenditure of time becomes even longer as manufacturers expand the instruments' triggering capability and memory size to increase the probability of localizing faults. This helps explain why they are not yet widely used in field-service or production applications where test time is often at a premium.

The need for simpler digital test equipment in field-service and production testing inspired Hewlett-Pack-



Fast service. Combining the best of two analyzer worlds, the model 532 captures 250 32-bit words of logic-state data and automatically computes and displays two associated signatures that identify faults in the microprocessor-based system under test.

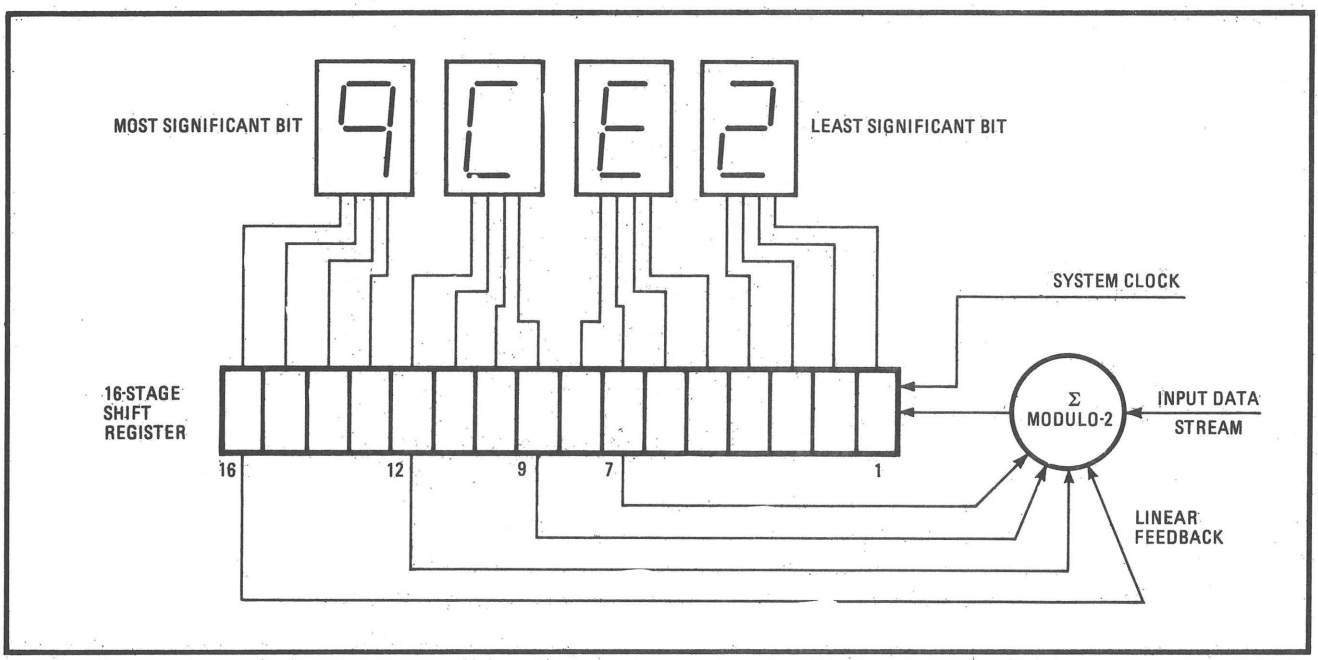


1. Localizing faults. In the basic logic-state analyzer, parallel data is clocked synchronously into a memory for later display in binary, hexadecimal, or octal notation. The instruments are widely used in monitoring sequential machine states and in software debugging.

ard's development of the model 5004A signature analyzer (Fig. 2). With a single-channel probe, this instrument captures a pulse train of digital events unique to the particular circuit node being examined. This pulse train, or serial bit stream, is fed to a linear-feedback shift register with tapped outputs driving a four-digit alphanumeric display. Each test node in a digital circuit thus is given an identifying four-character signature, much as each node in an analog circuit is characterized by an identifying voltage.

In operation, a series of signatures are computed for nodes in a known-good digital circuit and recorded on the corresponding schematic, in a troubleshooting guide, or even on the printed-circuit board itself. Circuit failures are isolated simply by moving the analyzer's probe from one test node to the next until the signature noted differs from the expected result. The component failure must be between the good and bad nodes. It is as simple as that, and a detailed understanding of circuit operation is not necessary at this point.

However, signature analysis currently works only for testing systems designed to accommodate it. For example, the system must supply a clock pulse to load the bit stream into the analyzer's shift register. It must also



2. Watching digits. In the basic signature analyzer, a single-channel probe catches a pulse train unique to the node under examination. Passing this train through a linear feedback register gives an identifying signature that can be compared with that of a known-good node.

A look at two signature-analysis algorithms

Signatures can be created from data streams using algorithms implemented in either hardware or software. The conventional single-channel signature analyzer employs a hardware technique based on a 16-bit linear-feedback shift register. The algorithm in the model 532 differs in two respects besides its implementation in software. It operates on parallel, rather than serial, data streams, and it operates on data that has already been collected, rather than in real time.

In the hardware approach, the feedback mechanism consists of a modulo-2 summation of selected taps of the shift register with the input serial data stream. This arrangement falls into the category of a cyclical redundancy check and is well documented in the literature of information theory.

Sampling signals that are supplied by the circuit under test precisely define the duration of the bit stream. When sampling is halted, a residue of the original serial data is left in the register. Because of the feedback, this residue, or signature, is as representative of events occurring at the beginning of the stream as it is of those at the end. [*Electronics*, March 3, 1977, p. 91.] To cite some of the error-detection properties of this technique:

- The probability is 1 (100%) that two identical serial bit streams will produce the same signature during testing.
- The probability is 0 that two serial bit streams will produce the same signature if they differ by precisely 1 bit.
- The probability is 2^{-16} or less that two serial bit streams will produce the same signature if one stream has multibit errors disclosed during testing.

For the software approach, the signature algorithm begins by zeroing the accumulator in the 532's microprocessor. The first word in the data memory is then added to the contents of the accumulator, generating a sum. The next word is added to this sum, generating a new sum plus a carry bit that is saved. This process, including adding in the carry, continues until all the data words contained in the memory have been processed. The final carry is discarded, and the resulting sum is a residue or signature of the memory contents.

Saving the carry at each step and adding it to the intermediate sum in the accumulator performs a function similar to the tapped bits in the linear-feedback shift register to the extent that this action ensures that all words in memory equally affect the outcome of the final signature. If the length of the data word is 16 bits, the error-detecting properties of the resulting four-digit signature are similar to those for the hardware approach.

supply specific start and stop signals so that the duration of the stream is defined and repeatable, and it must have provisions for exciting normally static nodes while breaking digital feedback paths in order to avoid signature ambiguities.

To accomplish this, the product's design must include special hardware and software to support the test instrument: something that may not be feasible when board or program space is at a premium. It is for this reason that the signature analyzer is not yet found in widespread use in the field.

Combining the two

The new model 532 logic-state and signature analyzer overcomes many of the problems of the two individual instruments. It computes two four-digit hexadecimal signatures after each data collection, one for each separately clocked 16-channel half of the analyzer's 32-bit-wide memory. After each collection, both 16-bit halves are processed, word by word, using a add-and-carry algorithm of the residue type (see "A look at two signature-analysis algorithms").

The resulting pair of four-digit hexadecimal signatures appears on the front-panel display of the instrument. Also, it can be written out on an oscilloscope, along with a 16-word page of data (Fig. 3). In much the same way that the single-channel signature analyzer converts a complex serial bit stream into an identifying four-digit code, the 532 compresses the entire contents of its 32-bit-by-250-word data memory (8,000 bits total) into two four-digit words.

For a given test setup, the memory will contain a specific, repeatable set of data for which a unique signature pair can be calculated. As long as the system under test is operating properly, this setup will continually yield the same signatures. Once even one bit of the entire set of collected data changes, the associated signature comes up differently.

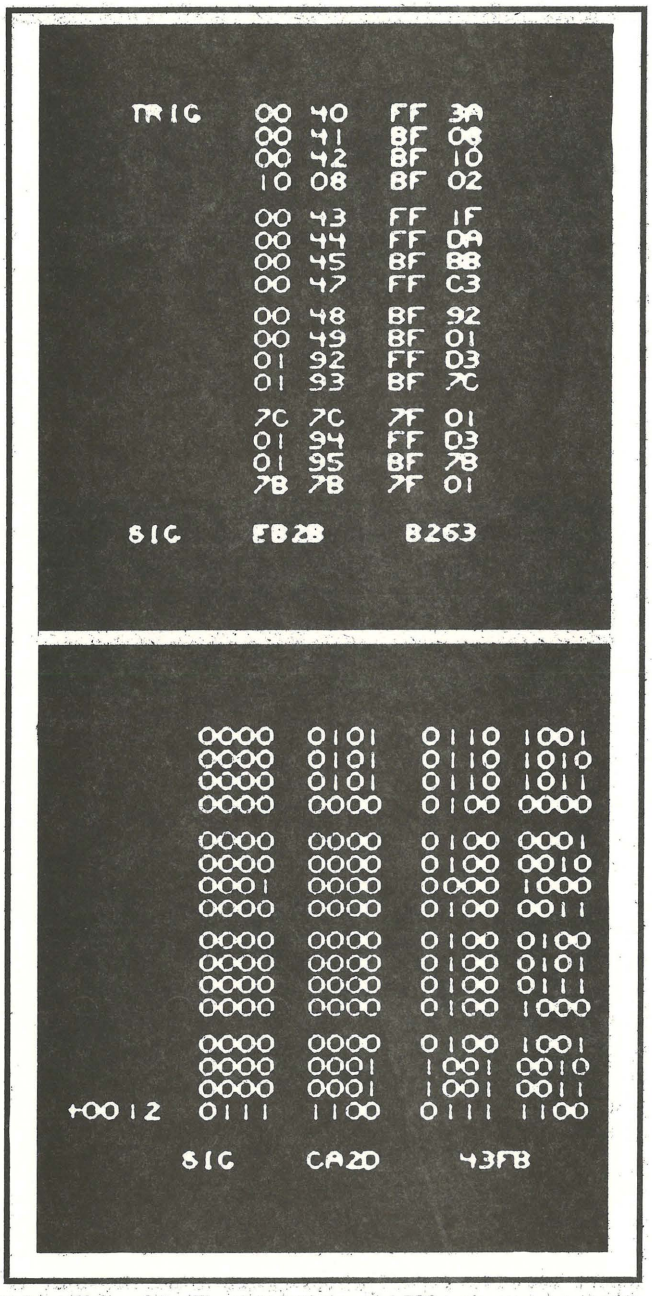
Since these signature calculations are performed on the data gathered by the 532 in its normal course of operation, no special hardware or software support features need be integrated into the system under test when it is designed. Also, the large amount of data collected by the instrument's memory, which would present a formidable analysis task for the user, is analyzed in a single stroke. This feature is particularly helpful when comparing sequential data collections in search of the problematic one.

The signature-analysis feature of the 532 can also be used to verify that the instrument itself is working properly. For example, it has a back-panel self-test port to accept the data-input probes. Each time the unit is turned on, a special routine is executed. If the resulting signatures are correct, the user is assured that the entire instrument is operational.

Operating the 532

A good example of the 532 in operation is a simple microprocessor-based controller. This unit is to be used in a relatively severe industrial environment, and it is the designer's job to determine if it will meet its performance specifications under simulated operating conditions. Random bursts of electromagnetic interference, variations in supply voltage, and changes in temperature are common examples of these conditions.

To assess the controller's susceptibility to operational failure, it is essential to view simultaneously as many critical signals as possible. In the test setup (Fig. 4), 32 signals are monitored: the 16-bit address bus, the 8-bit data bus, and eight status signals. The system is first



3. Identifying data. The data in the model 532 main memory can be displayed in the form of 16-word pages on a scope in hexadecimal (top) or binary (bottom), along with the identifying signatures.

operated under benign laboratory conditions to verify proper program execution and to compute a known-good signature pair. The designer need not calculate these signatures in advance, since the 532 does that. Thus, the measurement can be treated as empirical, just as it is when a signature analyzer is used alone.

With the expected four-digit codes recorded and the process controller's program in a loop mode, the designer can vary the environmental conditions while watching their effect on the displayed signatures. For example, a lowered supply voltage may increase the product's susceptibility to externally generated emi such that one or more of the data or status bits comes up in the wrong state. Then the associated signature will change.

Immediately the designer knows that the simulated environmental conditions are beginning to affect system performance, although the particular failure may not have been catastrophic. In fact, were it not for the use of logic-state signature analysis in the test setup, minor failures might even go unnoticed.

Adding auxiliary memory

In this controller example of a 532 at work, the sudden signature change indicates that a failure has occurred. What step of the program and which bit or bits of the associated data or status word are responsible? Without painstakingly recording and comparing the expected data with the erroneous collection, all the designer knows for sure is that an error has occurred. The location is still a question mark.

However, storing a set of known-good signatures and data in an auxiliary memory of the 532 turns precise identification of the problem area into a simple two-step process. The first is to capture data into the main memory from the system under test and compare the resulting signature pair with the expected values in the auxiliary memory. The instrument does this automatically, and any differences are flashed on the display. Once a difference is noted, the second step is a bit-by-bit comparison of the 8,000 bits of data in each of the two memories. Again, the 532 does this automatically, and any discrepancies are highlighted.

For example, if the failure is due to one of the status bits misbehaving in step 107 of the controller's program, the precise bit responsible is immediately evident. Investigating further, the designer might find that the corresponding address word, which is also displayed by the 532, has a number of lower-order bits change from all 1s to all 0s just as step 107 occurred. Perhaps the internally generated noise associated with the address transition has caused that particular status bit to fail. To find out, the analyzer's trigger output can trigger an oscilloscope on step 107 as the designer views the suspect circuitry with the scope's probes.

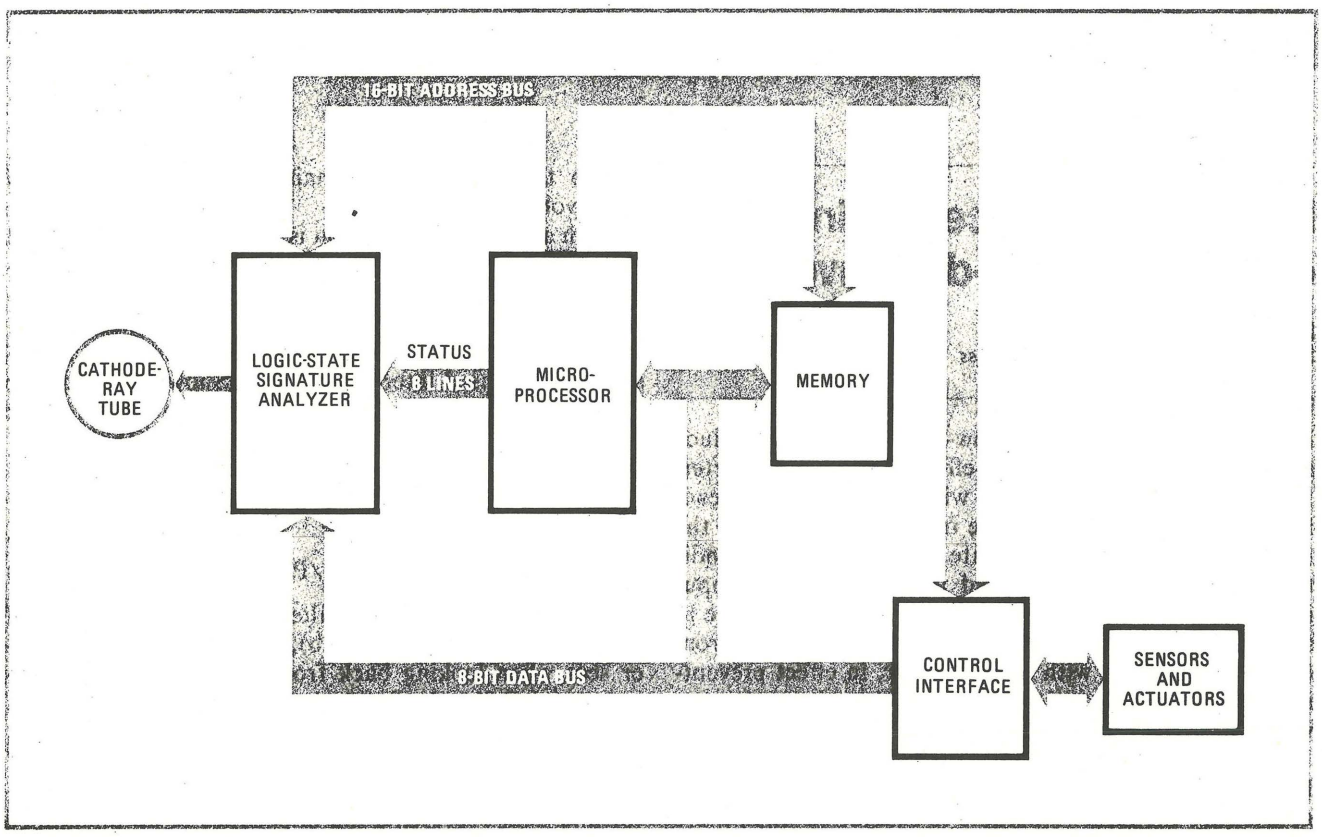
Using the 532 in the field

Combining auxiliary memory with logic-state analysis and signature analysis clearly makes the resulting instrument package more useful in field-service applications. This usefulness can be enhanced by a nonvolatile auxiliary memory that contains both the expected data and signature for a given application.

The 532's auxiliary memory incorporates seven programmable read-only-memory chips for nonvolatile storage, as well as a random-access memory for temporary storage. Each of these eight memory elements can store a complete 32-bit-by-250-word data collection and the corresponding signatures.

The contents of the main memory are transferred to the selected auxiliary memory element by a front-panel keystroke. In the case of the programmable ROMs, the instrument first checks to see if the selected device is blank before transferring the data and signature via internal programming circuitry.

Using this technique, the results of seven tests performed on a known-good system can be carried along



4. Checking a controller. In monitoring the performance of a microprocessor-based industrial controller, the 532 is first used with the product operating under laboratory conditions. Then it looks for signature changes as the environmental conditions are varied.

with the field engineer on a service call. To make the visit faster and easier, the 532 incorporates a learning mode in which the actual control settings used to collect the known-good data and signatures are automatically programmed into the auxiliary memory.

Replicating known-good data

When the field engineer wants to execute a particular test, the configuring of the instrument for that test—including setting up the triggering words, collection modes, clock or loop delays, etc.—is performed automatically. In this manner, he knows that the test performed on a known-good system can be replicated in the field. Otherwise there would be no positive way of knowing whether comparisons between field- and factory-generated data are truly valid.

The RAM in the auxiliary memory can also be useful in the field. If the seven basic tests in the PROMs are not enough to find the problem, additional tests may be down-loaded into the RAM over a telephone line, using a standard modem and the instrument's RS-232-C interface. Such a test would operate the same way as the tests in PROM. Test setup and execution are entirely automatic and under remote control. After new data is collected and compared with the stored values, the results of this comparison, including the associated signatures, can be sent back over the telephone line to the factory, which is better equipped to deal with difficult problems.

It has been said that it is sometimes easier to build a product than to test it. This is particularly true for microprocessor-based systems in which production test stations are complex setups that require highly trained personnel to operate them.

Where the logic-state analyzer and the signature analyzer may individually fail to satisfy the unique demands of the production-test environment, a combined instrument has a better chance for success. The logic-state signature analyzer offers a rapid go/no-go indication using its signature-analysis feature, automatic test execution, hardcopy output via its RS-232-C interface, and a broad monitoring capability of critical system signals. The 532 also includes an IEEE-488 interface for the execution of a series of production tests under the control of an external computer.

Circumventing limitations

The combined technique can circumvent some of the limitations of logic-state and signature analysis, particularly when teamed with an auxiliary memory. However, one should note that it is not as simple to use as the single-channel signature analyzer for finding a faulty component in a circuit.

The 532 is more of a general-purpose instrument in its analytic approach and does not rely on product-supplied hardware and software to support testing. Thus, bits flashing on the display will only have relevance for fault-isolation purposes to the user with an understanding of the circuitry involved. But, for a quick overview of system operation as well as an in-depth look into the complexities of the circuitry involved, the combination of logic-state and signature analysis is useful in a variety of test situations. □